# COE 202 – Digital Logic Design
# EE 200 – Digital Logic Circuit Design
# Syllabus for Term 081 – Fall 2008

Computer Engineering Department
College of Computer Sciences & Engineering
King Fahd University of Petroleum & Minerals

**Professor:** Muhamed Mudawar, Room 22/328, Phone 4642
**Office Hours:** SMW 11 am – 1 pm.
**Course URL:** http://faculty.kfupm.edu.sa/coe/mudawar/coe202/
**Email:** mudawar@kfupm.edu.sa

## Catalog Description

Introduction to information representation and number systems. Boolean algebra and switching theory. Manipulation and minimization of completely and incompletely specified Boolean functions. Physical properties of gates: fan-in, fan-out, propagation delay, timing diagrams, and tri-state drivers. Combinational circuit analysis and design, multiplexers, decoders, comparators, and adders. Sequential circuit analysis and design, basic flip-flops, clocking and timing diagrams. Registers, counters, RAMs, ROMs, PLAs, PLDs, and FPGAs.

**Prerequisite:** PHYS 102.

## Textbook

M. Morris Mano, *Digital Design*, *Third Edition*, Prentice Hall, 2002. ISBN: 0-13-035525-9.

## Online Lessons

Online lessons are available at http://faculty.kfupm.edu.sa/coe/mudawar/coe202/cd/index.htm with animation and sound. They are divided into six units with several lessons in each unit.

Unit I – Number System and Codes

Unit II – Binary Logic and Gates

Unit III – Combinational Logic

Unit IV – Sequential Circuits

Unit V – Registers and Counters

Unit VI – Memory and PLDs

## Course Learning Outcomes

- Carry out arithmetic computations in various number systems (binary, octal, hexadecimal).
- Apply rules of Boolean algebra to simplify Boolean expressions.
- Translate Boolean expressions into equivalent truth tables and logic gate implementations and vice versa.
- Design efficient combinational and sequential logic circuit implementations from functional description of digital systems.
- Carry out simple CAD simulations to verify the operation of logic circuits.

## Grading Policy

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| Assignments & Quizzes | 15% |
| Project | 10% |
| Major Exam I | 20% |
| Major Exam II | 25% |
| Final Exam | 30% |

- NO makeup will be given for missing quizzes or exams.

## Course Topics and Weekly Breakdown

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| 1 | Introduction, number system and arithmetic |
| 2 | Number base conversion, signed numbers and signed number arithmetic |
| 3 | Binary logic, basic identities, algebraic simplifications |
| 4 | Canonical and standard forms, physical properties of gates |
| 5 | Logic simplification using K-maps, K-map manipulation |
| 6 | 2-level and multi-level implementations, universal gates |
| 7 | Combinational logic and adders |
| 8 | Carry look-ahead adders and MSI components |
| 9 | Design with MSI components |
| 10 | Sequential circuits, latches and flip-flops |
| 11 | Design of Sequential circuits |
| 12 | Analysis of Sequential circuits |
| 13 | Registers and Counters |
| 14 | Programmable logic |