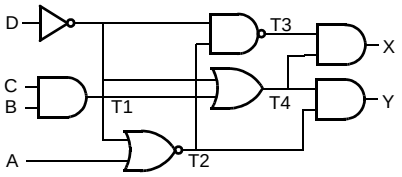
Problem Solutions to Problems Marked With a * in

Logic Computer Design Fundamentals, Ed. 2

CHAPTER 3

3-2.



$T1 = BC, \quad T2 = \overline{A}D$

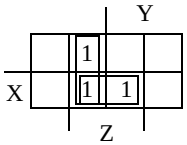
$T3 = 1, \quad T4 = \overline{D} + BC$

$X = T3T4$

$= \overline{D} + BC$

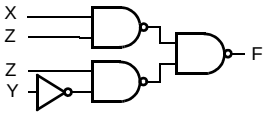
$Y = T2T4$

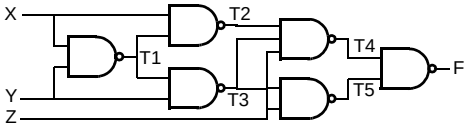
$= \overline{A}D(\overline{D} + BC) = \overline{A}\,BCD$



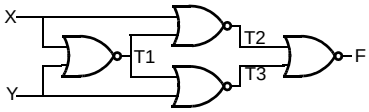
$XZ + Z\overline{Y}$

X	Y	Z	T1	T2	T3	T4	T5	F
0	0	0	1	1	1	1	1	0
0	0	1	1	1	1	0	0	1
0	1	0	1	1	0	1	1	0
0	1	1	1	1	0	1	1	0
1	0	0	1	0	1	1	1	0
1	0	1	1	0	1	1	0	1
1	1	0	0	1	1	1	1	0
1	1	1	0	1	1	0	0	1



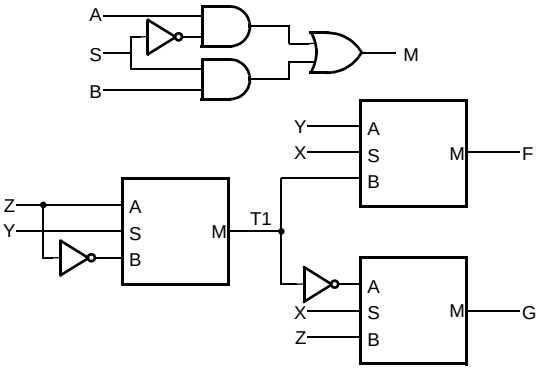


3-3.



X	Y	T1	T2	T3	F
0	0	1	0	0	1
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

3-6.



$M = A\overline{S} + BS$

$T_1 = Z\overline{Y} + \overline{Z}Y$

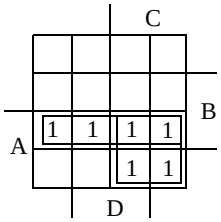
$F = Y\overline{X} + T_1X = Y\overline{X} + X(Z\overline{Y} + \overline{Z}Y)$

$= \overline{X}Y + X\overline{Y}Z + XY\overline{Z}$

$G = \overline{T}_1\overline{X} + ZX = XZ + \overline{X}(\overline{Z} + Y)(Z + \overline{Y})$

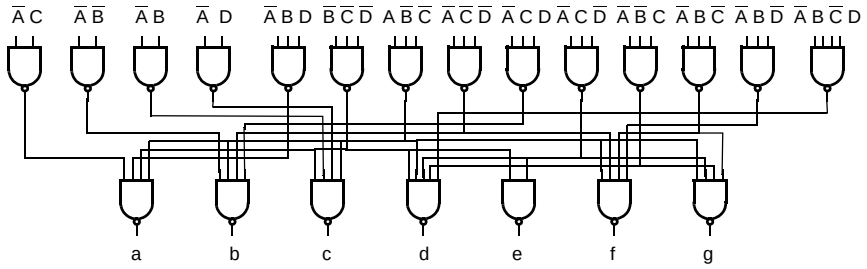
$= XZ + \overline{X}(YZ + \overline{Y}\,\overline{Z}) = XZ + \overline{X}YZ + \overline{X}\,\overline{Y}\,\overline{Z}$

3-11.

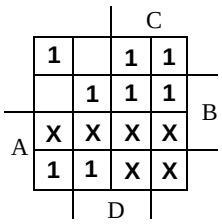


$F = AB + AC$

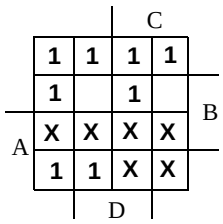
3-13.



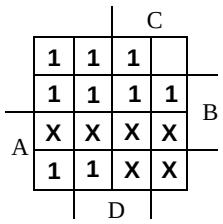
3-15.



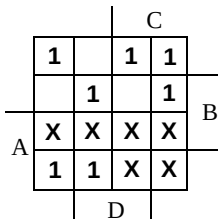
$a = A + C + BD + \bar{B}\,\bar{D}$



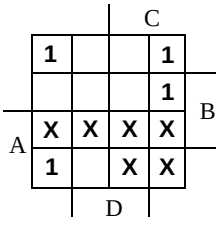
$b = \bar{B} + \bar{C}\,\bar{D} + CD$



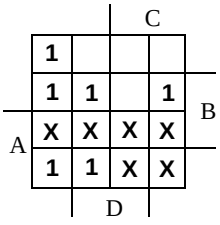
$c = B + \bar{C} + D$



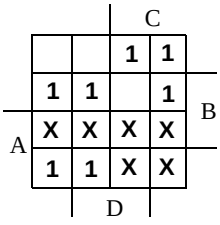
$d = B\bar{C}D + A + \bar{B}\,\bar{D} + \bar{B}C + C\bar{D}$



$e = \bar{B}\,\bar{D} + C\bar{D}$



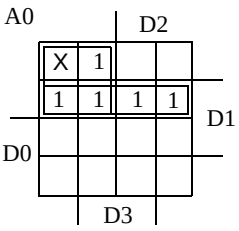
$f = A + B\bar{D} + B\bar{C} + \bar{C}\,\bar{D}$

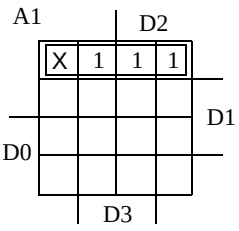


$g = A + C\bar{D} + \bar{B}C + B\bar{C}$

3-20.

D3	D2	D1	D0	A1	A0	V
0	0	0	0	X	X	0
X	X	X	1	0	0	1
X	X	1	0	0	1	1
X	1	0	0	1	0	1
1	0	0	0	1	1	1



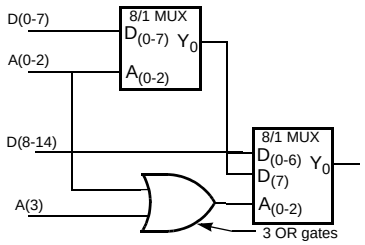


$V = D0 + D1 + D2 + D3$

$A0 = D1 + \overline{D0}\;\overline{D2}$

$A1 = \overline{D0}\;\overline{D1}$

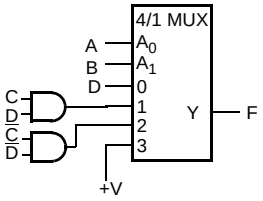
3-25.



3-29.

A	B	C	D	F	
0	0	0	0	0	
0	0	0	1	1	D
0	0	1	0	0	
0	0	1	1	1	
0	1	0	0	1	$\overline{C}\,\overline{D}$
0	1	0	1	0	
0	1	1	0	0	
0	1	1	1	0	

A	B	C	D	F	
1	0	0	0	0	CD
1	0	0	1	0	
1	0	1	0	0	
1	0	1	1	1	
1	1	0	0	1	+V
1	1	0	1	1	
1	1	1	0	1	
1	1	1	1	1	



3-35.

$$C_1 = \overline{T_3 + T_2} = \overline{T_1\overline{C}_0 + T_2} = \overline{\overline{A_0B_0}\,\overline{C_0} + \overline{A_0 + B_0}} = \overline{(\overline{A}_0 + \overline{B}_0)\overline{C}_0 + \overline{A}_0\overline{B}_0} = (A_0B_0 + C_0)(A_0 + B_0)$$

$$C_1 = A_0B_0 + A_0C_0 + B_0C_0$$

$$S_0 = C_0 \oplus T_4 = C_0 \oplus T_1\overline{T}_2 = C_0 \oplus \overline{A_0B_0}(A_0 + B_0) = C_0 \oplus (\overline{A}_0 + \overline{B}_0)(A_0 + B_0) = C_0 \oplus A_0\overline{B}_0 + \overline{A}_0B_0$$

$$S_0 = A_0 \oplus B_0 \oplus C_0$$

3-38.

1	0	0	1	1	0	0	0	1	0	0	1	1	0	0	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	1	1	0	0	1	1	1	0	1	1	0	0	1	1	0	0	1	0	1	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
0	1	1	0	1	0	0	0	0	1	1	0	0	1	1	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

3-41.

+43	=	0101011	43		0101011
-17	=	1101111	+(–17)	+	1101111
-43	=	1010101			10011010
+17	=	0010001	= 26	=	0011010
			–43		1010101
			+ 17	+	0010001
			= –26	=	1100110

3-45.

	S	A	B	C4	S3	S2	S1	S0
a)	0	0111	0110	0	1	1	0	1
b)	0	0100	0101	0	1	0	0	1
c)	1	1100	1010	1	0	0	1	0
d)	1	0101	1010	0	1	0	1	1
e)	1	0000	0010	0	1	1	1	0

3-49.

78430258 98989899 09580089 99999999

3-52.

BCD

	A	B	C	D	E	F	G	H
0	0	0	0	0	1	0	0	1
1	0	0	0	1	1	0	0	0
2	0	0	1	0	0	1	1	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	0	1
5	0	1	0	1	0	1	0	0
6	0	1	1	0	0	0	1	1
7	0	1	1	1	0	0	1	0
8	1	0	0	0	0	0	0	1
9	1	0	0	1	0	0	0	0

$H = \overline{D}$

$G = C$

$F = \overline{B}C + B\overline{C}$

$E = \overline{A}\overline{B}\overline{C}$

Gates: 8

Literals: 9

EXCESS-3

	A	B	C	D	E	F	G	H
0	0	0	1	1	1	1	0	0
1	0	1	0	0	1	0	1	1
2	0	1	0	1	1	0	1	0
3	0	1	1	0	1	0	0	1
4	0	1	1	1	1	0	0	0
5	1	0	0	0	0	1	1	1
6	1	0	0	1	0	1	1	0
7	1	0	1	0	0	1	0	1
8	1	0	1	1	0	1	0	0
9	1	1	0	0	0	0	1	1

$H = \overline{D}$

$G = \overline{C}$

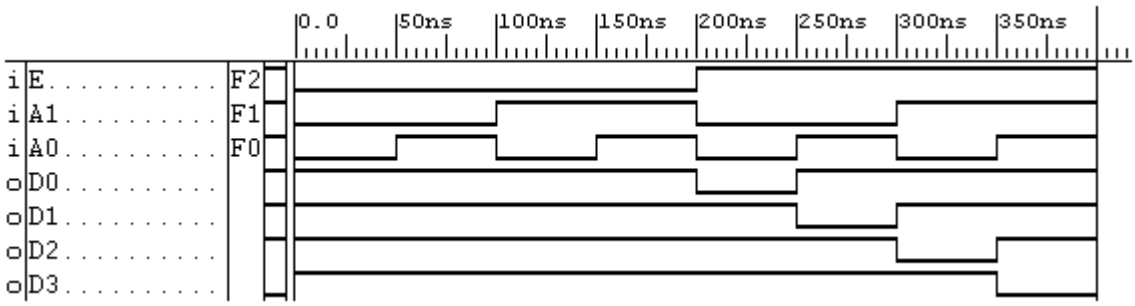
$F = \overline{B}$

$E = \overline{A}$

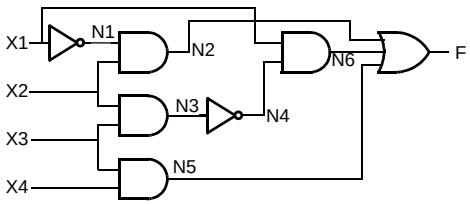
Gates: 4

Literals: 4

3-55.



3-58.



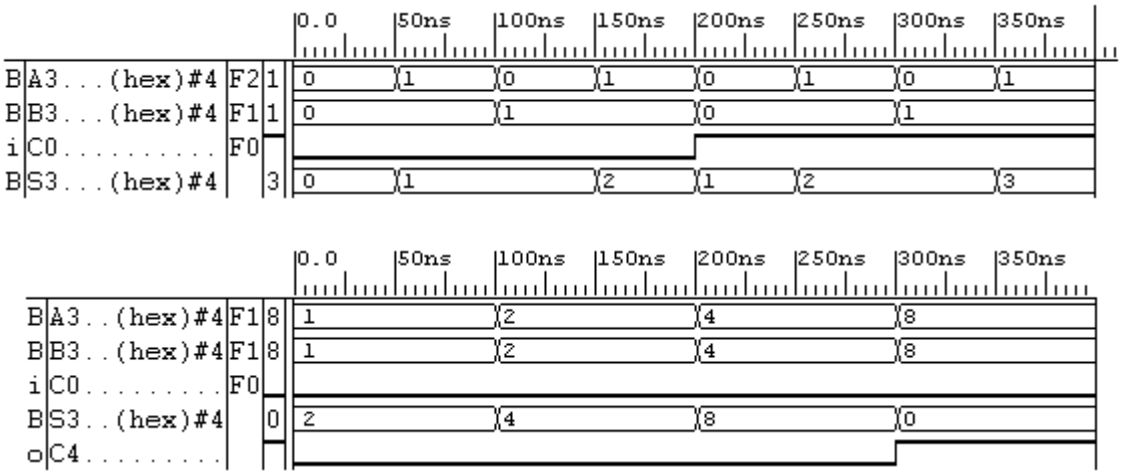
3-62.

From 3-2: F = X Z + Z $\overline{Y}$

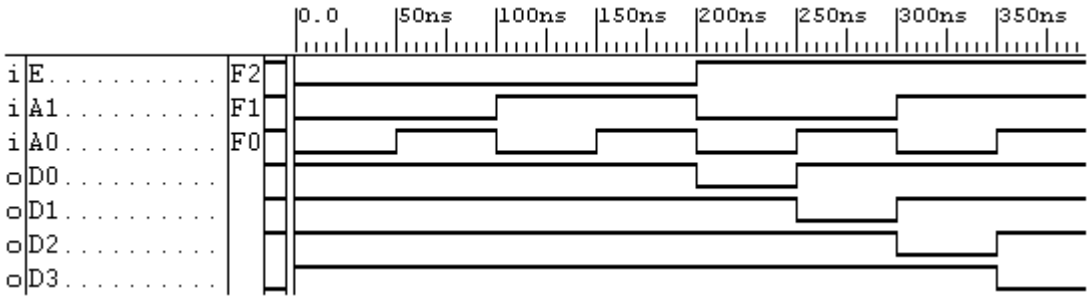
Using Nand Gates:

```
...
signal T: std_logic_vector(0 to 2);
begin
  g0: NOT1 port map (Y, T(0));
  g1: NAND2 port map (X, Z, T(1));
  g2: NAND2 port map (Z, T(0), T(2));
  g3: NAND2 port map (T(1), T(2), F);
 end
```

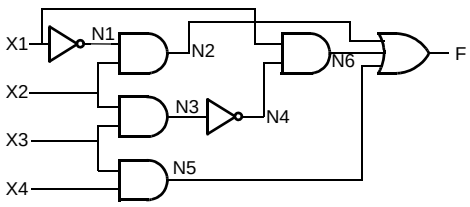
3-66.



3-69.



3-72.

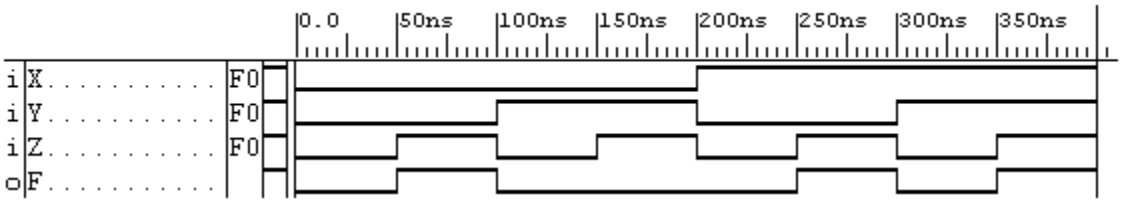


3-76.

```
//Fucntion F from problem 3-2 =  X Z + Z Y

module cicuit_3_76(X, Y, Z, F);
  input X, Y, Z;
  output F;

  assign F = (X & Z) | (Z & ~Y);
endmodule
```



3-80.