RFID Beginner's Kit
Command Reference Manual

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4. Tags

4.1. Overview of supported tags

	Serial Number	Page Read	Page Write	Transfer Mode
I•CODE®	yes	yes	yes	not applicable
TagIt®	yes	yes	yes	not applicable
TagIt® ISO 15693	yes	yes	yes	yes
My-d® SRF55V10P	yes	yes	yes	yes
My-d® SRF55V02P	yes	yes	yes	yes
My-d® SRF55VxxS	yes	planned	planned	planned
ISO15693	yes	yes	yes	yes
MIFARE Classic	yes	not supported	not supported	partial
MIFARE Pro, Pro X	yes	not supported	not supported	planned
MIFARE Light	yes	not supported	not supported	not supported
MIFARE Ultra Light	yes	yes	yes	yes
SLE66CL160S (A)	yes	not supported	not supported	planned
SLE66CL160S (B)	yes	not supported	not supported	yes
ISO14443A	yes	not supported	not supported	yes
ISO14443B	yes	not supported	not supported	planned
ISO14443C	yes	planned	planned	yes
SRF176	yes	yes	yes	yes

4.2. ISO 15693

The reader can communicate with ISO 15693 tags. An anticollision has to be performed if multiple instances of tags are in an energizing field. The reader detects the different types of ISO 15693 labels and can handle them individually. All commands are supported for these tags. Leading character to identify these tag type is ‘V’

4.2.1. My-D Label

My-D labels are specific labels of Infineon. Two different modes of tags are supported: plain and secure mode. At the moment only plain mode tags are supported in full functionality. The serial number of all secure tags is readable.

4.2.1.1. Memory organization of SRF55VxxP

Two vicinity integrated circuit cards (VICC) with 320 byte or 1k byte EEPROM memory are available. The EEPROM memory is divided into pages. Each page consists of 8 byte for data storage and 2 byte for administrative purpose.
The EEPROM of **SRF55V10P** is organized in **128 pages** addressed 00hex to 7Fhex. The EEPROM of **SRF55V02P** consists of **32 pages** addressed 00hex to 1Fhex.

Notation: hexadecimal bytes, x denotes nibble (4 bit) of any value
The term "page" is used as a synonym for "block" in this document.

	Byte address (hex)	**Byte number within page**									**Administrative Area**	
											RFU	Access Condition
		0	1	2	3	5	5	6	7		8	9
User Area	7F	User Data									55	AA
	7E	User Data									55	AA
	...	..									..	..
	..	..									..	..
	1F	User Data									55	AA
	..	..									..	..
	..	..									..	..
	05	User Data									55	AA
	04	User Data									55	AA
	03	User Data									55	AA
Service Area	02										55	76
	01										55	66
	00	Unique Identification Number									55	46

Table 4-1: Memory organization of SRF55VxxP labels

4.2.1.2. User Area

SRF55V10P – 125 pages of 8 byte
SRF55V02P – 29 pages of 8 byte

4.2.1.3. Administrative Area

Byte 9 defines access condition of each page. Read only is coded as 66hex and Write/Read as 0xAA.

4.2.1.4. Service Area

Page 00 contains the **Unique Identification Number** (UID) of the VICC. The number is set by the IC-manufacturer according ISO/IEC 15693-3. The number is unique for each single IC within the ISO/IEC world and cannot be changed. The UID is needed for the **anticollision procedure**. Page 01 and 02 are reserved for IC internal functions. The whole Service Area is **Read only**

64 57	56 49	48 41	40 1
'X110 0000'	**IC mfr code**	**IC manufacturer serial number**	
'E0' or '60'	'05'	Chip ID byte	Unique Number

Table 4-2:Coding of UID

The MSB of the UID can be either '0' or '1' shown as 'X' above.

4.2.1.5. Chip ID Byte

Bit 48 to bit 41 of the UID is defines according Table 4-3

Bit 48	47	46	45	44	43	42	41
EEPROM Size			Security Bit	Chip Type			

Table 4-3: Coding of bit 48 to bit 41 – EEPROM memory size

The EEPROM memory size is defines as following

Code	**Description**	**Comment**
000	10 kBit	SLE55V10
001	5 kBit	
010	2,5 kBit	SLE55V02
011	1,25 kBit	
100	20 kBit	
101	r.f.u.	Reserved for future use
11x	r.f.u.	Reserved for future use

Table 4-4: EEPROM memory size

4.2.1.6. Security Bit

Bit 45 of UID

'1'	Chip supports Crypto Security mechanism
'0'	Chip supports Plain Mode only

Table 4-5: Coding of bit 45 – Security bit

4.2.1.7. Chip Type

Code	Description
0000	55Vxx chip functionality
0xxx	Backwards compatible to 55Vxx functionality
1xxx	Reserved for future use

Table 4-6: Coding of bit 44 to 41 – Chip Type

Note:

The Chip Type should be check to make sure to work with an chip out of the 55Vxx family. Bit 44 should be '0' that means at least backward compatibility of new more powerful ICs of the 55 product family.

4.2.2. Tagit ISO

The physical memory structure is byte oriented and is organized in blocks of fixed size as shown in Table 4-7: Tagit ISO memory structure.

Block #	32 Bit				Lock bits	
					F	U
1						
2						
3						
…		…			…	
…		…			…	
62						
63						
64						
UID 1						
2						
DSFID						
AFI						
Mem & IC Ref	0x81 IC Ref		0x03 Block Size	0x3F # of Blocks	Factory	

Table 4-7: Tagit ISO memory structure

The available user memory is separated in 64 blocks 32 bits each. This results in 2 Kbits available user memory.

4.2.2.1. Additional blocks

- UID: factory programmed. Universal identification number
- Mem & IC Ref: IC Ref is the current version of the tag, block size and number of blocks. both are interpreted as value + 1.
- DSFID: user programmable field to store the DSFID number. see ISO 15693 for further information.
- AFI: user programmable field to store the AFI value. see ISO 15693 for further information.

4.2.2.2. Locks

User data can be locked. This feature is not supported from the reader at moment. The UID is factory lock and cannot be changed. This number is used to identify all tags in the ISO 15693 world. Additionally the block size and the number of available blocks is set in the factory and cannot be changed.

4.3. ISO 14443

The reader can only handle single tags according ISO 14443 type A or B. The reader can identify a single tag and returns its serial number. The leading character is 'M' in both protocols. This character is used to identify and separated different tags.

All other command such as read, write, select are not supported.

The Mifare® transponder family consists of various 13.56 MHZ transponders IC, all according to ISO 14443 (Identification cards – Contactless integrated circuit(s) cards – Proximity cards).

The ISO 14443 consists of the following four parts

Part 1 Physical characteristics
Part 2 Radio frequency and signal interface
Part 3 Initialization and anticollision
Part 4 Transmission Protocols

4.3.1. Mifare® standard tags

The Mifare® standard tag consists of 16 sectors. Each sector has four blocks. Each block has 16 bytes.

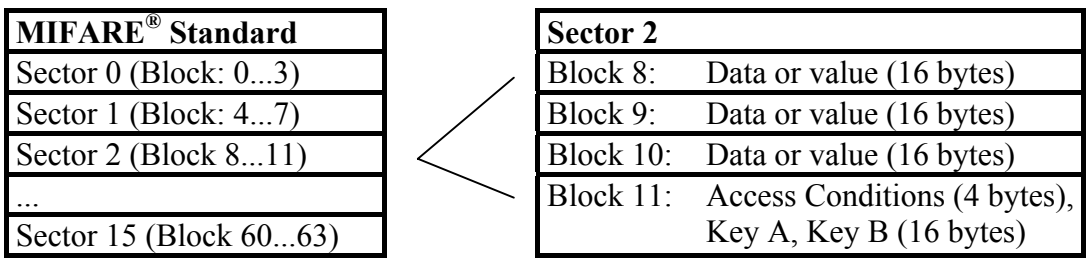

Table 4-8: Memory of Mifare® Standard tag

4.3.1.1. Sector 0 / Block 0

Serial Number (4 byte)	Check byte (1 byte)	Manufacturer data (11 byte)

Table 4-9: Block 0 at Sector 0

Serial number is factory locked and read only.

4.3.1.2. Block 3, 7, 11, 15, …

Key A (6 byte)	Access Conditions (4 bytes)	Key B (6 byte)

Table 4-10: Organization of Access Condition/ Key blocks

Transport keys (keys after manufacturing, on delivery):
Key A: A0 A1 A2 A3 A4 A5 (Infineon) or FF FF FF FF FF FF (new Philips cards)
Key B: B0 B1 B2 B3 B4 B5 (Infineon) or FF FF FF FF FF FF (new Philips cards)
Access Conditions: FF 07 80 xx (key A used to read or write, the key A itself is not readable; key B is data only)

Note
Using key B as data area will cause a security gap, due to the fact that it is necessary to rewrite key A and Access Conditions at every write access (Mifare® does only support read/write whole blocks). Therefore, this configuration is not recommended for security sensitive applications.

4.4. Mifare Ultra Light

4.4.1. Memory organization

Byte Name	0	1	2	3	Page
Serial Number	SN0	SN1	SN2	BCC0	0
Serial Number	SN3	SN4	SN5	SN6	1
Internal/ Lock	BCC1	Internal	Lock0	Lock1	2
OTP	OTP0	OTP2	OTP3	OTP4	3
Data	Data0	Data1	Data2	Data3	4
Data	Data0	Data1	Data2	Data3	5
Data	Data0	Data1	Data2	Data3	6
Data	Data0	Data1	Data2	Data3	7
Data	Data0	Data1	Data2	Data3	8
Data	Data0	Data1	Data2	Data3	9
Data	Data0	Data1	Data2	Data3	A
Data	Data0	Data1	Data2	Data3	B
Data	Data0	Data1	Data2	Data3	C
Data	Data0	Data1	Data2	Data3	D
Data	Data0	Data1	Data2	Data3	E
Data	Data0	Data1	Data2	Data3	F

Table 4-11: Memory organization of Mifare Ultra Light

Note:
Bold frame indicates User Arena. Read/Write access depends on Lock0/ Lock1 bits.

4.4.2. UID/ Serial Number

The unique serial number consists of 7 bytes and is stored in two pages. First part is placed on page 0, second on page 1. Check Bytes (BCC) are needed to fulfill ISO 14443-3. The UID is factory programmed and cannot be changed.

Page 0			
SN0	SN1	SN2	BCC0

Page 1			
SN3	SN4	SN5	SN6

Page 2			
BCC1	Internal	Lock0	Lock1

Table 4-12: UID/ Serial Number description

Note:
Anticollision Cascade level A only responds first part of UID. Second level anticollision has to be performed in order to received whole UID (7 Bytes). See section 2 for detailed information.

4.4.3. Lock Bytes

The bits of Byte 2 and 3 of page 2 represents the field programmable locking mechanism.

Each page from 3 to F may be locked to prevent further write access. Figure

MSB		Lock Byte 0				LSB	
L 7	L 6	L 5	L 4	L OTP	BL 15-10	BL 9-4	BL OTP

MSB		Lock Byte 1				LSB	
L 15	L 14	L 13	L 12	L 11	L 10	L 9	L 8

Table 4-13: Lock Bytes

Lx locks one page to Read Only.
BLx blocks further locking of the memory area x

Note:
Single bits area set with normal write command. If a block lock bit is set according lock bits cannot be changed anymore. **This procedure is irreversible**.

4.4.4. OTP Bytes

Page 3 contains OTP bits. All bits are factory programmed to 0.

			Page 3
OTP0	OTP1	OTP2	OTP3

Table 4-14: OTP Byte description

Bits in OTP bytes are “or”-ed together. Once a bit is set to 1 it cannot be changed back. Bits are set with the normal write command.

Note:
This memory area may be used as a 32 ticks one-time counter.

4.4.5. Data Bytes

Page 4 to F are user area. It can be changed according write access as defined in lock bits. For write and read commands see section 2

4.4.6. Command set

4.4.6.1. State diagram

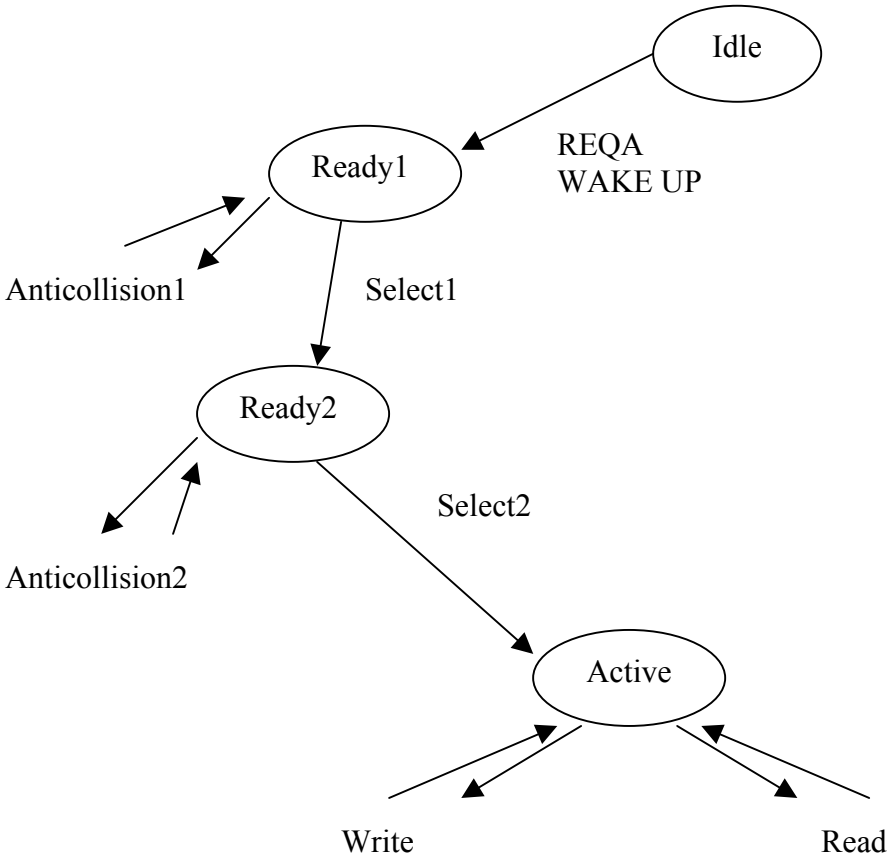

Figure 4-1: State Diagram

The state diagram shows the different state of a Mifare Ultra Light transponder. All activating and selecting procedures are done with a high level select command. This sophisticated procedure is needed to identify a tag uniquely.

4.5. I•Code

The I•Code label is designed for long range applications. The data is stored in a non-volatile EEPROM. Its capacity is 512 bits organized in 16 blocks consisting 4 bytes each (1 block = 32 bits). First 4 blocks contain the serial number, write conditions and some configuration bits. The memory organization is shown in Table 4-15.

	Byte 0	Byte 1	Byte 2	Byte 3	
Block 0	SNR0	SNR1	SNR2	SNR3	Serial number
Block 1	SNR4	SNR5	SNR6	SNR7	Serial number
Block 2	F0	FF	FF	FF	Write access conditions
Block 3					Special Functions (EAS)
Block 4					Family code Identifier
Block 5					User Data
Block 6					…
Block 7					…
Block 8					…
Block 9					…
Block 10					…
Block 11					…
Block 12					…
Block 13					…
Block 14					…
Block 15					…
Block 16					User Data

Table 4-15: I•Code memory organization

4.5.1. Serial number

The serial number of a label is programmed during the developing process. It is stored on block 0 and block 1. SNR0 shown in Table 4-15 represents the least significant byte and SNR7 the most significant.

4.5.2. Write Access Conditions

Block 2 contains the write access condition for each of the 16 blocks. A bit can be set to 0 which means write protections. Each block can be locked with that procedure including block 2. Protecting block 2 involves a permanently lock of the write access conditions.

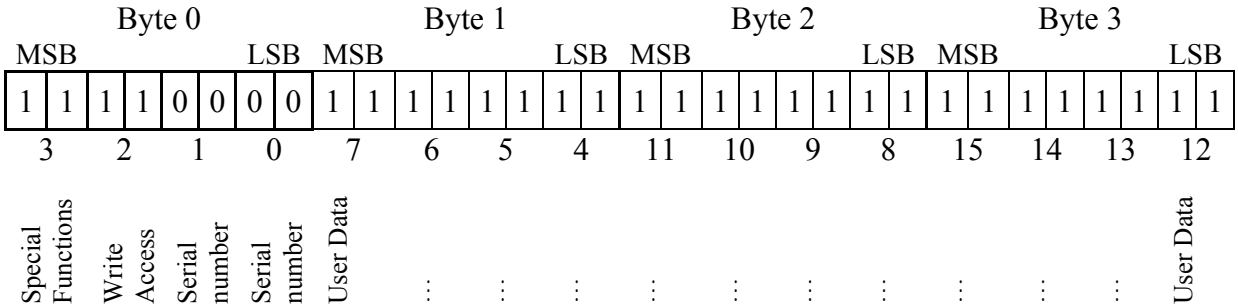

Figure 4-2: I•Code Write Access Condition bytes

It is important to change always both bits. Only 11 (write access enable) or 00 (write protected) are allowed.

Note:
Be extremely careful when changing write access in block 2. In a case of a mistake you might loose write access to all blocks of a label.

Special Functions (EAS)and Family Code/Application Identifier are additional features and are not listed in details.

All other blocks are **User Data** and can be changed according the state of the Write Access Conditions.

4.6. TAGIT

TAGIT labels include information of block numbers and block size. The reader automatically detects the correct memory organization. Using command 'T' the reader returns the serial number of a label. Additionally two byte containing the block size and block number of recently used label are displayed.

Note:
Using continuous read command the reader will only return the serial number of a label without block size and block number information.

4.7. SR167

4.7.1. Memory organization

Block Address	MSB B15	16 bits Block b8 b7	LSB B0	Description
0	UID 0			64 bit UID ROM
1	UID 1			
2	UID 2			
3	UID 3 (fixed: D002)			
4	User Area			EEPROM Lockable
5	User Area			
6	User Area			EEPROM Lockable
7	User Area			
8	User Area			EEPROM Lockable
9	User Area			
A	User Area			EEPROM Lockable
B	User Area			
C	User Area			EEPROM Lockable
D	User Area			
E	User Area			EEPROM Lockable
F	OTP Lock_Reg	Reserved	Chip_ID	

Table 4-16: Memory organization of SR176

Each page of the memory has 2 bytes. The UID is stored in the first four pages and are factory locked. The UID is stored in the memory as follows.

b63															b0
b15	UID 3				b0	b15	UID 2			b0	b15	UID 1		b0	b15	UID 0	b0

All other pages can be locked according the settings of Lock_Reg.

4.7.2. Lock_Reg

Row 15 bits	bits	bit description
b15	Lock_Reg b7	Block 14 & 15 lock status
b14	Lock_Reg b7	Block 12 & 13 lock status
b13	Lock_Reg b7	Block 10 & 11 lock status
b12	Lock_Reg b7	Block 8 & 9 lock status
b11	Lock_Reg b7	Block 6 & 7 lock status
b10	Lock_Reg b7	Block 4 & 5 lock status
b9	Lock_Reg b7	Block 2 & 3 lock status
b8	Lock_Reg b7	Block 0 & 1 lock status
b4 to b7	b0 to b3	Reserved
b0 to b3	Chip_ID b0 to b3	Chip_ID

Table 4-17: Lock_Reg

The Lock_Reg register is designed as OTP register. If a bit is set this blocks will be set as ROM.