| ID | | Task Name | Duration | Start | Finish | Predecessors | Resource Nam |
|---|---|---|---|---|---|---|---|
| | | **Prepare an action plan** | **days** | **Tue / /** | **Mon / /** | | **Group** |
| | | **Problem analysis and survey of different options** | **days** | **Tue / /** | **Wed / /** | | **Group** |
| | | **System Design and Segmentation** | **days** | **Sat / /** | **Sun / /** | | **Group** |
| | | **Design of the Control unit** | **days** | **Tue / /** | **Tue / /** | **, , ,** | |
| | | **Selection of a control scheme** | **days** | **Mon / /** | **Wed / /** | | **Ahmad** |
| | | **Logic Design of CU** | **days** | **Sat / /** | **Tue / /** | | **Ahmad** |
| | | **FPGA synthesis of CU** | **days** | **Wed / /** | **Mon / /** | | **Ali** |
| | | **CU Testing** | **days** | **Tue / /** | **Mon / /** | | **Ali** |
| | | **Design of the execution unit** | **days** | **Tue / /** | **Tue / /** | | |
| | | **Data path design** | **days** | **Tue / /** | **Mon / /** | | **Ahmad** |
| | | **Design of the register file** | **days** | **Wed / /** | **Mon / /** | | **Ali** |
| | | **Design of the Bus arbitration Unit** | **days** | **Wed / /** | **Mon / /** | | **Ahmad** |
| | | **Design of the TLB unit** | **days** | **Sun / /** | **Sat / /** | | **Ali** |
| | | **Integration of the EU** | **days** | **Tue / /** | **Mon / /** | **, ,** | **Ali** |
| | | **System Integration** | **days** | **Tue / /** | **Tue / /** | **,** | **Group** |
| | | **Testing and Debuging** | **days?** | **Wed / /** | **Wed / /** | | **Group** |
| | | **Final Report** | **days** | **Sat / /** | **Sat / /** | | **Group** |