COE360 – Assignment # 9 (out of 20)
Dr. M. Elrabaa (052) (individual submission)

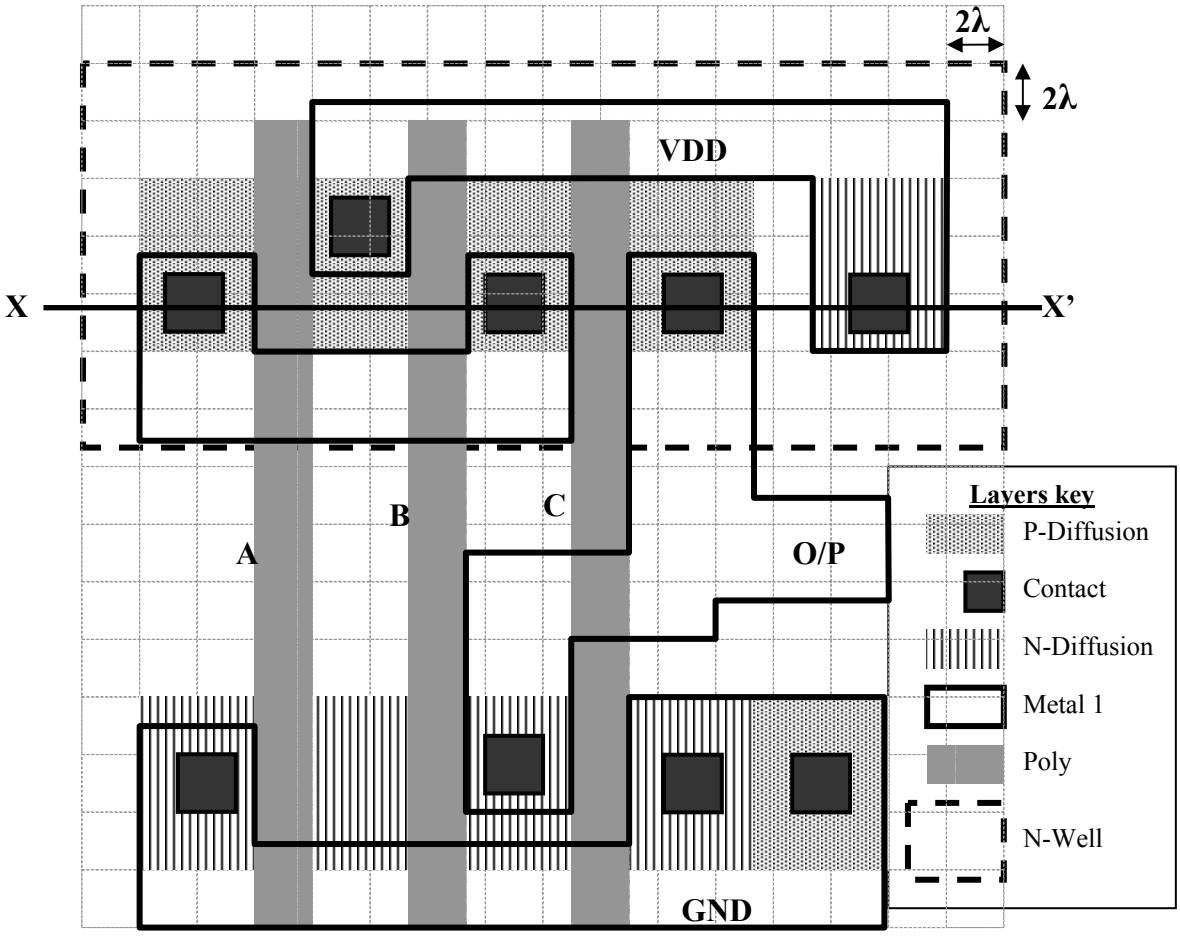
Use a 1 µm technology with V_{DD}=5V, C_{ox}=2 fF/µm^2, ϵ_{rox}= 4, ϵ_{rSi}= 12, ϵ_o= 8.85E-14 F/cm, μ_n=600 cm^2/S·V, μ_p=300 cm^2/S·V, $I_{Dsat_{nmos}}$= 500 µA/µm, $I_{Dsat_{pmos}}$= 250 µA/µm, $V_{tn} = |V_{tp}|$ = 0.8 V, and q=1.6E-19 C.

No group submission will be accepted for this assignment!

Q1) Design a non-inverting (i.e. with even number of stages) CMOS buffer chain with an input capacitance of 35 fF to drive a load of 3.5 pF with minimum delay and equal noise margins and rise and fall delays.

Q2) The following layout is of a CMOS circuit:

1. **Obtain the circuit schematic with transistors sizes (W/L) in microns (assume a 1µ m technology)**
2. **What is the function of this circuit?**
3. **Draw a crossection showing all the layers along the line X-X'**



Q3) Obtain the symbolic layout of an AOI 122 CMOS gate then draw the layout in Magic. Make all NMOS and PMOS transistors equal in size. Use the following formula to obtain Wn (then set Wp=2 Wn): Wn = your student ID # Mod 7

i.e. Divide your student ID# by 7 then take the remainder as Wn. E.g. if your student ID is 281234 then take 281234/7 = 40176.28571 → Wn = 0.28571 * 7 = 2 µm. If you get a Wn below 1µm, then just use 1µm.