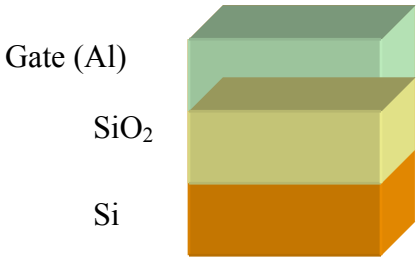
COE 360 – 2nd Assignment – Dr. Muhammad Elrabaa

1. The gate capacitance of an MOS device with an Aluminum gate, Silicon substrate and SiO_2 insulator was measured to be $3X10^{-7}$ F/cm^2. Also its threshold was measured to be –0.6 V:
   (a) What is the oxide thickness?
   (b) Assuming that the oxide trapped charge is zero, what is the substrate type? Calculate the substrate doping.
   (c) Redo (b) above with an oxide trapped charge of 10^{-7} cm^{-3}.

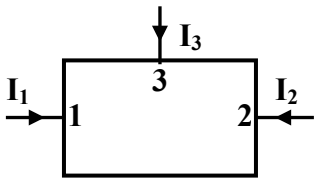
Hint: Get the constants you need from the text book, chapter 3. You can solve the resulting non-linear equations by hand (iterations) or write a simple program to do that. **[3 marks]**



2. An MOS transistor is made with a P-Type Polysilicon gate and an N-type Silicon substrate ($N_D=10^{15}$ cm^{-3}). The oxide thickness is 20nm and the oxide trapped charge is -5E-8 c/cm^2.
   (a) Calculate the threshold of this device and determine its type,
   (b) Calculate the required substrate doping to make the threshold -0.8V **[2 marks]**

3. For the MOS transistor (shown in the figure below) the following measurements were made using the three terminals shown in the figure (none of them is the substrate):

Terminal Voltages			Terminal Currents		
V_1	V_2	V_3	I_1	I_2	I_3
0 V	0 V	0 V	0 mA	0 mA	0 mA
1 V	0 V	0 V	1 mA	-1 mA	0 mA
0 V	1 V	0 V	-1 mA	1 mA	0 mA
2 V	1 V	0 V	0 mA	0 mA	0 mA
1 V	2 V	0 V	0 mA	0 mA	0 mA
2 V	1 V	1 V	1 mA	-1 mA	0 mA



- Current into a terminal is positive
- Current out of a terminal is negative

a. Which terminal is the gate?

b. What is the type of this transistor (NMOS or PMOS)?

c. What is the range of possible values of the threshold voltage? Is this a depletion mode or enhancement mode transistor? **[2.5 marks]**

4. Fill the following table showing the effects (increase, decrease or no effect) of certain process/operating conditions on an enhancement PMOS Source-to-drain current. Also give a brief explanation of why these effects would take place: [2.5 marks]

Process/Operation condition	Effect on I_{SD}	Explanation
Higher Substrate doping		
Lower Temperature		
Thicker Gate Oxide		
A more positive Oxide trapped charge		
A larger gate-metal′s work function		