COE 561, Term 081

Digital System Design and Synthesis

Course Project

The list of course projects proposed for this term are as shown below. In each project, the main objective of the project and the expected team members are specified. Each student must select a project according to the deadlines specified below.

1. Reliability-Driven Don't Care Assignment for Two-Level Logic Synthesis [2 Students]

Recently, two algorithms have been proposed for the selective assignment of don't cares to enhance the reliability of two-level logic circuits. The algorithms use a Hamming-distance based metric to determine 0/1 assignments for the most critical don't care terms, thereby leaving flexibility in the circuit specification for subsequent area minimization. In this project, the students will implement the two algorithms and generate results on benchmark circuits based on running espresso, SIS, and reliability analysis based on simulations.

2. Reliability-Driven Don't Care Assignment for Multi-Level Logic Synthesis [2 Students]

Recently, an efficient algorithm was proposed for computing Complete Don't-Care (CDC) set based on Satisfiability (SAT)-based computation algorithm and windowing. This algorithm is implemented in ABC synthesis tool. In this project, the students are required to understand the implemented algorithm and be able to manipulate the implemented code. The purpose of this is to be able to manipulate the derived don't care conditions before using them for simplification.

3. Reliability-Driven State Assignment for Sequential Logic Synthesis [2 Students]

It is well known that state assignment has an impact on the area, performance, power and testability of synthesized circuits. In this project, students will evaluate the impact of state assignment on the reliability of synthesized sequential circuits. Monte Carlo simulation-based reliability analysis will be implemented by the students. Based on experimental analysis students are expected to develop a metric to guide state assignment for enhancing reliability. Students will also modify a given implementation of a genetic-based state assignment algorithm for enhancing circuit reliability.

4. Implementation of ITE DAG [2-3 students]

In this project, the students will implement the ITE procedure and display the obtained ITE DAG in a graphical format. The input to this procedure is the three functions f, g, and h. It can be assumed that these functions will be specified in two-level format either in equation or PLA format. The tool will also accept the variable order to be used in the implementation of the ITE DAG. The output will be the reduced ITE DAG. Since this tool is meant for educational purposes, the student is required to have a debugging option where he displays the execution

steps of the algorithm in a user friendly format to allow students to follow the algorithm execution.

5. Heuristic-Based Two-Level Logic Minimization Based on Covering [2-3 students]

In this project, the students will implement heuristic based two-level minimization based on solving a covering problem heuristically. First, the prime implicants of a two-level function will be computed based on the studied procedure. Then, the problem will be formulated as a covering problem and solved heuristically after applying matrix reduction procedures including essential columns, row dominance and column dominance. Then, a column will be selected based on the highest number of rows covered. Input to the developed tool is assumed to be in PLA format. The student will generate results on benchmark circuits and compare their obtained solution with espresso exact and espresso heuristic algorithms.

6. Design of a Digital Circuit from a Behavioral Description [2 students]

In this project, the students are required to select a design problem and model the behavior of the circuit to be designed in either Verilog or VHDL. The students are then required to use Synopsys Behavioral Compiler to design two circuits targeting area and speed. They should verify that the synthesized solution captures the required behavior of the designed circuits. Working on this project requires prior knowledge of either Verilog or VHDL and learning Synopsys synthesis tool.

Project Deadlines:

Task	Deadline
Project selection	Tuesday, Dec. 23
Project Plan	Tuesday, Dec. 30
Progress Report	Tuesday, Jan. 13
Final Report & Project Demonstration	Tuesday, Jan. 27

Each student group is expected to submit a project plan describing the project tasks, the time planned for each task, and the team members' role in each task. Each group is also required to submit a progress report describing briefly the progress made so far in the project against planned work, difficulties faced, results obtained so far and the tasks to be performed in the next period. At the end of the project, each group is required to submit a professional report showing the details of all the work performed and demonstrate their project to me.

Project Evaluation Criteria:

Task	Mark
Project Plan	5%
Progress Report	10%
Project Accomplishments vs. Requirements	60%
Final Report Documentation & Organization	25%