COE 561, Term 081
Digital System Design and Synthesis
HW# 3

Due date: Sunday, Jan. 4

Q.1. Consider the following function:

$$X = A\,B\,E\,G' + A\,B\,F\,G + A\,B\,E'\,G + A\,C\,E\,G' + A\,C\,F\,G + A\,C\,E'\,G + D\,E\,G' + D\,F\,G + D\,E'\,G$$

(i) Compute all the kernels of X using the recursive kernel computation algorithm. Show all the steps.

(ii) Compute all the kernels of X based on matrix representation. Compare your answer to the result obtained in (i).

(iii) Find a quick factor of X by using the first level-0 kernel found. Assume that input variables are sorted in lexicographic order. Determine the number of literals obtained. Compare your solution with the result obtained by running the sis commands ***factor –q x; print_factor; print_stats –f.***

Q.2. Consider the following function:

$$X = A\,C\,D\,E + B\,C\,D\,E + A'\,B'\,F\,G + A'\,B'\,F'\,G' + E\,C\,F + E\,C'\,G + E'\,C\,F' + E'\,C'\,G'$$

(i) Compute all double-cube divisors of X along with their bases and their weights. Show only double-cube divisors that have non-empty bases.

(ii) Apply the fast extraction algorithm based on extracting double-cube divisors along with complements or single-cube divisors with two-literals. Show all steps of the algorithm. Determine the number of literals saved. Compare your solution with the result obtained by running the sis commands ***fx***.

Q.3. Consider the logic network defined by the following expressions:

$$X = AC + B;$$
$$Y = X + A'\,B;$$
$$Z = Y\,C';$$

Inputs are {A, B, C} and output is {Z}.

(i) Compute the SDC set for node X.

(ii) Using the SDC set of node X, simplify the function Y.

(iii) Compute the ODC set for node Y.

(iv) Simplify the function of Y using both its ODC and SDC of node X.

(v) Apply the sis command ***full_simplify*** and compare the solution obtained with your obtained solution based in (iv).

Q.4. Consider the logic network defined by the following expressions:

$k = a \cdot b$

$l = a \cdot c$

$h = a + c$

$e = a' + b$

$g = k + l$

$f = d' \cdot g$

$i = f \oplus d$

$x = e \oplus i$

$j = f + d$

$y = j + h$

Inputs are {a, b, c, d} and outputs are {x, y}. Assume that the delay of each inverter, AND and OR gates is 1 and that the delay of each XOR gate is 2. Also, assume that the input data-ready times are zero except for input a, which is equal to 2.

(i) Draw the logic network graph and compute the data ready times and slacks for all vertices in the network.

(ii) Determine the **maximum propagation delay** and the **topological critical path**.

(iii) Suggest an implementation of the function ***g*** in terms of the Inputs *{a, b, c}* to reduce the delay of the circuit. What is the **maximum propagation delay** after the modified implementation?