(viii) **VHDL Model**

```
library ieee;
use ieee.std_logic_1164.all;


entity hw2 is
port (a,b, c, d:in std_logic; f:out std_logic);
end hw2;
architecture  behav of hw2 is
begin
f <=     (not(a) and not(b) and not(c) and not(d))OR
   (not(a) and not(b) and not(c) and  d)OR
   (not(a) and not(b) and  c and not(d))OR
   (not(a) and  b and not(c) and not(d))OR
   (not(a) and  b and not(c) and  d)OR
   (not(a) and  b and  c and not(d))OR
   (not(a) and  b and  c and  d)OR
   ( a and not(b) and not(c) and not(d))OR
   ( a and not(b) and not(c) and  d)OR
   ( a and not(b) and  c and not(d))OR
   ( a and  b and not(c) and  d)OR
   ( a and  b and  c and not(d))OR
   ( a and  b and  c and  d);
end behav ;
```

Using Design Compiler and library and_or.lib with default constraints, we get the following circuit: