COE 561, Term 051

Digital System Design and Synthesis

HW# 1

Due date: Sunday, Oct. 2

Q.1. It is required to model an **n-bit Carry Look-Ahead Adder**. The adder receives two n-bit inputs **A**, **B** and a Carry-in signal, **Cin**, and produces an n-bit output **C** representing the sum, a carry out signal, **Cout**, and the signal **OV** indicating if an overflow occurs or not. It is assumed that numbers are represented using 2's complement representation. Note that OV is 1 if the result performed on signed numbers is incorrect. Use type **bit** and **bit_vector** for the signals used in your models.

(i) Describe an Entity **4CLADDER** in VHDL for a 4-bit carry look-ahead adder.

(ii) Model in VHDL Architecture, **Concurrent,** for modeling this 4-bit carry look-ahead adder using **concurrent** statements. Simulate the VHDL model **Concurrent** and verify that it is working properly. Include a snapshot of the simulated waveform.

(iii) Describe an Entity **CLADDER** in VHDL for a n-bit carry look-ahead adder. Assume that the size of the adder is specified as a **generic** parameter.

(iv) Model in VHDL Architecture, **Structural,** for modeling this n-bit adder at the structural level using generate statements. Simulate the VHDL model **Structural** and verify that it is working properly for an **8-bit adder**. Include a snapshot of the simulated waveform.

Q.2. It is required to model a sequence detector that detects the sequence 11011 assuming overlapping sequence detection.

(i) Design the FSM for detecting this sequence assuming overlapping sequences.

(ii) Model your FSM design in VHDL using a **behavioral model** assuming **rising-edge** triggering and **asynchronous** reset.

(iii) Model a test bench that tests the behavior of the sequence detector generating the CLK input with a clock period of 100ns with 50% duty cycle, and the input sequence 00110101110110110010111011100.