KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COLLEGE OF COMPUTER SCIENCES & ENGINEERING

COMPUTER ENGINEERING DEPARTMENT

COE 561: Digital System Design and Synthesis
Syllabus - Term 182

Catalog Description

Overview of modern digital systems; Systems-on-chip, virtual cores, design reuse and IP's (soft, firm and hard), ASIC design methodologies. Digital system hierarchy & abstraction levels, Hardware Modeling using HDL, Design optimization and performance criteria, HDL coding for synthesis, Testability of digital systems and High-Level synthesis.

Pre-requisite: Graduate Standing

Instructor Dr. Aiman H. El-Maleh Room: 22/407-5 Phone: 2811
Email: aimane@kfupm.edu.sa

Office Hours *UMTW 11:00-12:00 PM, and by appointment*

Reference Books

1. Zainalabedin Navabi, "VHDL: Analysis and Modeling of Digital Systems", McGraw-Hill, Inc.
2. Giovanni De Micheli, "Synthesis & Optimization of Digital Circuits," McGraw Hill

Grading Policy

Assignments	20%	
Literature Review	10%	
Project	20%	
Midterm Exam	20%	**(Sat. March 9, 10:00 AM)**
Final	30%	

- Attendance will be taken regularly. Excuses for officially authorized absences must be presented no later than one week following resumption of class attendance.
- Late assignments will be accepted with a penalty of 10% per each late day.
- A student caught cheating in any of the assignments will get 0 out of 15%.

- No makeup will be made for missing Exams.

Detailed Syllabus

1.	Microelectronics, semiconductor technologies, microelectronic design styles, ASIC design methods, design representations, levels of abstraction & domains, Y-chart, system synthesis and optimization, issues in system synthesis. Systems-on-a-chip using Cores, Core Types: Soft Cores, Firm Cores, Hard Cores.	**~ 1.5** Week
2.	Combinational and Sequential Circuit Design: Boolean Expansion Based on Orthonormal Basis, Iterative Arithmetic Combinational Circuits, Sequential Circuit Design Procedure, State Minimization, State Encoding, Retiming, Sequential Circuit Timing.	**~ 2** Weeks
3.	Design of a digital system by partitioning it into a Data Path and Control unit -- Design of DP and CU. Algorithmic State Machine (ASM) charts.	**~ 3** Weeks
4.	Introduction to design using VHDL synthesizable code.	**~ 3** Weeks
5.	Field Programmable Gate Arrays (FPGAs), FPGA technologies, Design and synthesis with FPGAs, FPGA Memory Implementation, LUT-Based RAMS, Block RAM.	**~ 1.5** Weeks
6.	Synthesis of combinational and sequential logic: Introduction to synthesis, synthesis of combinational logic, Multilevel Logic Synthesis, Area and Delay estimation, Timing Issues in Multiple-Level Logic Optimization, Synthesis & Testability, Power Dissipation, Power Reduction Techniques, Design for Testability.	**~ 2.5** Weeks
7.	High-Level Synthesis (Design vs Synthesis, CFG, DFG, Sequencing Graph, Algorithms for Scheduling, Binding & Allocation)	**~ 1.5** Weeks