COE 561 Digital System Design and Synthesis
Term 081
Paper Presentation Evaluation

Name: _____

ID: _____

	Paper Title	Presenter Name	Paper Understand. (4)	Ability to Explain (4)	Present. Organizat. (2)	Total (10)
1	Enhancing Design Robustness with Reliability-aware Resynthesis and Logic Simulation	Abdulaziz Tabakh				
		Ayed Al-Qahtani				
2	On the Role of Timing Masking in Reliable Logic Circuit Design	ZAID ZURAIGAT				
		TAMEEM AL-MANI				
3	Seamless Integration of SER in Rewiring-Based Design Space Exploration	Orwa Diraneyya				
		Isah Lawal				
4	N-Variant IC Design: Methodology and Applications	Ahmad AlRefai				
		Wael Al Takrouri				
5	A Variation Aware High Level Synthesis Framework	Mohammed Asif				
		Irfan Khan				
6	A Heterogeneous CMOS-CNT Architecture utilizing Novel Coding of Boolean Functions	MAHER KAMAL				
		AHMAD ALI				