KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT
COE 561: Digital System Design and Synthesis
Term 051 Lecture Breakdown

	Date	Topics	Ref.
1	U 11/9	Syllabus, Introduction.	Chapter 1
2	T 13/9	**Introduction**: Microelectronics Design Problems, Microelectronics Design Styles, Design Domains & Levels of Abstraction, Digital System Design Process.	Chapter 1
3	U18/9	Design vs. Synthesis, Digital system design cycle, Design space and evaluation space, Pareto Optimality, **Introduction to VHDL**: Styles in VHDL, VHDL Terms, VHDL Models, Design Entity and Architecture, Examples: Full-Adder, One's Count Circuit.	Chapter 1 & Handout
4	T 20/9	VHDL Examples: 2x1 MUX, D-FF, Counter, Sequence Detector, Structural 4-bit Comparator, FOR..GENERATE Statement. Introduction to Modelsim HDL simulator.	Handout
5	U 25/9	IF..Generate Statement, Design Parameterization using Generic Statement, Test bench Example, VHDL Predefined Operators, Variables vs. Signals, Data flow Model: Unconditional, Conditional and Selected Signal Assignments, Block Statement, Process Statement.	Handout
6	T 27/9	Process Statement, Wait Statement, IF-Statement, Case Statement, Loop Control, For Loop, While Loop, Generalized VHDL Mealy & Moore Models. **Logic Synthesis Background**: Boolean Algebra, Boolean Functions, Shannon's Theorem.	Handout & 2.5
7	U 2/10	Unate functions, Boolean difference, Consensus, Smoothing, Orthonormal Basis Expansion, Representation of Boolean functions, **Binary Decision Diagrams.**	2.5
8	T 4/10	Reduced Binary Decision Diagrams, **ITE DAGs**, **Satisfiability**, **Minimum Covering Problem, Branch & Bound Algorithm**.	2.5
9	T 11/10	Covering reduction strategies, Exact Cover, Two-level minimization definitions, PLA minimization, **Positional cube notation**, Operations on logic covers: cofactor.	2.5 & Chapter 7
10	W 12/10	Sharp, Disjoint Sharp, Consensus, Computation of all prime implicants, Tautology, Containment,	Chapter 7

		Complementation.	
11	T 18/10	**Exact two-level minimization**, ESPRSSSO-EXACT, **Heuristic minimization**, Heuristic minimization operators: Expand, Reduce, Irredundant, Reshape.	Chapter 7
12	W 19/10	Expand heuristics, Reduce heuristics, Irredundant Cover.	Chapter 7
13	T 25/10	Irredundant Cover, Essentials, **Espresso algorithm**, Espresso Tool, Testability properties of two-level logic, Logic Network, Network optimization, Area Estimation.	Chapter 7 & 8
14	W 26/10	**Mutlilevel transformations**: Elimination, Decomposition, Factoring, Extraction, Simplification, Substitution. Elimination algorithm , **Algebraic model**, Algebraic division algorithm, Substitution algorithm, Extraction, Kernels.	Chapter 8
15	U 13/11	**Kernel Set Computation**, Recursive Kernel Computation, Matrix Representation of Kernels, Single-Cube Extraction, Multiple-cube extraction, **Decomposition**.	Chapter 8
16	T 15/11	**Factorization** Algorithm: quick & Good Factoring, **Fast Extraction** Algorithm: Double-cube divisors and single-cube divisors, Boolean Methods, Controllability & Observability don't care conditions.	Chapter 8
17	U 20/11	**Major Exam I.**	Chapter 8
18	T 22/11	**Satisfiability don't care** conditions, Controllability don't care computation, Observability don't care conditions computation.	Chapter 8
19	U 27/11	Transformations with don't cares, Optimization and perturbations, synthesis and testability, **Synthesis for testability,** timing issues in multilevel logic optimization, **delay modeling**, topological critical path.	Chapter 8
20	T 29/11	False path problem, Algorithms for delay minimization, Transformations for delay reduction, More refined delay models, Speedup algorithm	Chapter 8
21	U 4/12	**Library Binding**: Rule-based library binding, Algorithms for library binding, Partitioning, Decomposition, Matching, Covering, Tree-based matching.	Chapter 10
22	T 6/12	**Tree-based covering, Minimum Delay Cover**: constant and load-dependent delays, **Boolean matching**: Signatures and Filters.	Chapter 10
	Th 8/12	**Sequential Logic Synthesis**: Modeling Synchronous circuits, **State minimization** for completely-specified FSMs, State minimization for incompletely-specified FSMs: maximal compatible	Chapter 9

		classes, formulation of state minimization problem.	
23	U 11/12	Computation of Prime Compatibility Classes. Another state minimization example. **State Assignment**. State encoding for two-level models.	Chapter 9
24	T 13/12	Symbolic minimization, **Input encoding problem**, Dichotomy theory, Exact & Heuristic input encoding.	Chapter 7 & 9
25	U 18/12	**Output and mixed encoding**, Covering and Disjunctive relations, State encoding for two-level implementation, Synchronous logic network, **Retiming**.	Chapter 7 & 9
26	T 20/12	**Architectural-level synthesis**, Data-flow graphs, **Sequencing graphs**, Behavioral optimization of sequencing graphs.	Chapter 3 & 4
27	U 25/12	Synthesis in the temporal domain: **Scheduling**, Synthesis in the Spatial domain: **Binding**, Approached to Architectural Optimization, Scheduling Models, Minimum latency unconstrained scheduling, ASAP & ALAP scheduling, Latency Constrained Scheduling, Scheduling Under detailed timing constraints: minimum and maximum timing constraints.	Chapter 4 & 5
28	T 27/12	Scheduling under Resource Constraints, ILP Formulation, List scheduling for minimum latency under resource constraints.	Chapter 5
29	U 1/1	**List Scheduling** Algorithm for Minimum Resource Usage, **Force-Directed** List Scheduling , Force-Directed Scheduling Algorithm for Minimum Resources, Scheduling graphs with alternative paths.	Chapter 5
30	T 3/1	Allocation and Binding, Algorithmic Solution to the Optimum Binding Problem, Left-Edge Algorithm, ILP Formulation of Binding, Register Binding Problem.	Chapter 6