KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT
COE 561: Digital System Design and Synthesis
Term 101 Lecture Breakdown

Lec.#	Date	Topics	Ref.
1	U 26/9	Syllabus, **Introduction**: Microelectronics Design Problems, Microelectronics Design Styles.	Chapter 1
2	T 28/9	Microelectronics Design Styles, Dealing with design complexity, Design domains and levels of abstractions, Digital system design, Design vs. synthesis.	Chapter 1
3	U 3/10	Digital system design cycle, Synthesis process, High-level synthesis, Design and evaluation space, Combinational design space example, Architecture design space example, Pareto Optimality. **Logic Synthesis Background**: Boolean Algebra, Boolean Functions, Shannon's Theorem.	Chapter 1 & 2.5
4	T 5/10	Unate functions. Boolean difference, Consensus, Smoothing, Orthonormal Basis Expansion. Representation of Boolean functions, **Binary Decision Diagrams.**	2.5
5	U 10/10	Reduced Binary Decision Diagrams, **ITE DAGs**.	2.5
6	T 12/10	Applications of ITE DAGs. **Satisfiability**, Satisfiability Formulation as Zero-One Linear Programming (ZOLP) Problem, Minimum Covering Problem, Minimum-Vertex Cover Example, Minimum-Edge Cover Example, Covering Problem Formulated as Satisfiability Problem. **Branch & Bound Algorithm**. Covering reduction strategies. Branch and Bound Exact Covering Algorithm, Bounding function.	2.5
7	U 17/10	**Two-level minimization**: Programmable Logic Arrays. Minimal or irredundant cover, Minimal cover w.r.t. 1-implicant containment. Prime implicant, Prime cover, Essential prime implicant. **Positional cube notation**, Operations on logic covers: intersection, supercube, distance, cofactor, Sharp. Disjoint Sharp, Consensus, Computation of all prime implicants.	Chapter 7
8	T 19/10	Tautology, Containment. Complementation. **Exact two-level minimization**, ESPRSSSO-EXACT. **Heuristic minimization**, Heuristic minimization operators: Expand, Reduce, Irredundant, Reshape.	Chapter 7
9	U 24/10	Expand heuristics.	Chapter 7
10	T 26/10	Expand heuristics, Reduce, Irredundant.	Chapter 7

	Th 28/10	**Major Exam I**	
11	U 31/10	Irredundant, Essentials. Espresso Algorithm. Testability of Two Level circuits.	Chapter 7
12	T 2/11	Logic Network, Network optimization, Area Estimation. **Mutlilevel transformations**: Elimination, Decomposition, Factoring. Extraction, Simplification, Substitution. Elimination algorithm. **Algebraic model**. Algebraic division algorithm.	Chapter 8
	W 3/11	**Last day dropping with W**	
13	U 7/11	Substitution algorithm, Extraction, Kernels, Kernels computation. **Kernel Set Computation**, Recursive Kernel Computation.	Chapter 8
14	T 9/11	Kernels computation. **Kernel Set Computation**, Recursive Kernel Computation, Matrix Representation of Kernels. Single-Cube Extraction, Multiple-cube extraction.	Chapter 8
	11-26/11	**Eid Al-Adha Vacation**	
15	U 28/11	Value of a Kernel. **Decomposition**. **Factorization** Algorithm: quick & Good Factoring. **Fast Extraction** Algorithm: Double-cube divisors and single-cube divisors.	Chapter 8
16	T 30/11	Irredundant Procedure (revisited). **Fast Extraction** Algorithm: Double-cube divisors and single-cube divisors.	Chapter 8
17	U 5/12	Boolean Methods, Controllability & Observability don't care conditions. **Satisfiability don't care** conditions, Controllability don't care computation. Observability don't care conditions computation. Multi-Way Stems Theorem.	Chapter 8
18	T 7/12	Observability Don't Care Algorithm, Transformations with don't cares. Optimization and perturbations. Synthesis and testability.	Chapter 8
	Th. 9/12	**1ˢᵗ Paper Presentation**	
19	U 12/12	Synthesis and testability, **Synthesis for testability**. Timing issues in multilevel logic optimization, **delay modeling**, topological critical path. False path problem.	Chapter 8
	U 12/12	**Last day dropping all courses with W**	
20	T 14/12	Algorithms for delay minimization, Transformations for delay reduction. More refined delay models, Speedup algorithm. **Library Binding**: Library Models, Major Approaches, Rule-based library binding.	Chapter 8 & 10
21	U 19/12	Algorithms for library binding, Partitioning, Decomposition, Matching, Covering. Tree-based matching. **Tree-based covering. Minimum Area Cover, Minimum Delay Cover**: constant delay.	Chapter 10
22	T 21/12	**Minimum Delay Cover**: load-dependent delays,	Chapter 10

		Boolean matching: Signatures and Filters.	
	Th 23/12	**Major Exam II**	
23	U 26/12	**Sequential Logic Synthesis**: Modeling Synchronous circuits, **State minimization** for completely and incompletely-specified FSMs.	Chapter 9
24	T 28/12	No Class.	
25	U 2/1	**State minimization** for incompletely-specified FSMs. **State Assignment**. State encoding for two-level models. Symbolic minimization, **Input encoding problem.**	Chapter 7 & 9
26	T 4/1	Dichotomy theory, Exact & Heuristic input encoding. **Output and mixed encoding**, Covering and Disjunctive relation. State encoding for two-level implementation.	Chapter 7 & 9
27	U 9/1	Limitation of Symbolic Minimization and Constrained Encoding, Synchronous logic network, **Retiming**.	Chapter 9
	U 9/1	**Dropping all courses with WP/WF**	
28	T 11/1	**Architectural-level synthesis**, Data-flow graphs, **Sequencing graphs**, Behavioral optimization of sequencing graphs. Synthesis in the temporal domain: **Scheduling**, Synthesis in the Spatial domain: **Binding.** Scheduling Models, Minimum latency unconstrained scheduling, ASAP & ALAP scheduling, Latency Constrained Scheduling, Scheduling under Resource Constraints.	Chapter 3 & 4
	Th. 13/1	**2nd Paper Presentation**	
29	U 16/1	ILP Formulation, List Scheduling Algorithm for Minimum Latency, List Scheduling Algorithm for Minimum Resource Usage.	Chapter 5
30	T 18/1	Algorithmic Solution to the Optimum Binding Problem, ILP Formulation of Binding, Register Binding Problem. Left-Edge Algorithm.	Chapter 6