KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT
COE 561: Digital System Design and Synthesis
Term 091 Lecture Breakdown

Lec.#	Date	Topics	Ref.
1	U 4/10	Syllabus, **Introduction**: Microelectronics Design Problems, Microelectronics Design Styles.	Chapter 1
2	T 6/10	Dealing with design complexity, Design domains and levels of abstractions, Digital system design, Design vs. synthesis, Digital system design cycle, Synthesis process.	Chapter 1
3	U 11/10	High-level synthesis, Design and evaluation space, Combinational design space example, Architecture design space example, Pareto Optimality. **Logic Synthesis Background**: Boolean Algebra, Boolean Functions.	Chapter 1 & 2.5
4	T 13/10	Shannon's Theorem. Unate functions. Boolean difference, Consensus, Smoothing, Orthonormal Basis Expansion.	2.5
5	U 18/10	Representation of Boolean functions, **Binary Decision Diagrams.** Reduced Binary Decision Diagrams, **ITE DAGs**.	2.5
6	T 20/10	**ITE DAGs**. Applications of ITE DAGs. **Satisfiability**, Satisfiability Formulation as Zero-One Linear Programming (ZOLP) Problem, Minimum Covering Problem, Minimum-Vertex Cover Example, Minimum-Edge Cover Example, Covering Problem Formulated as Satisfiability Problem.	2.5
7	U 25/10	**Branch & Bound Algorithm**. Covering reduction strategies. Branch and Bound Exact Covering Algorithm, Bounding function. **Two-level minimization**: Programmable Logic Arrays.	2.5 & Chapter 7
8	T 27/10	Minimal or irredundant cover, Minimal cover w.r.t. 1-implicant containment. Prime implicant, Prime cover, Essential prime implicant. **Positional cube notation**, Operations on logic covers: intersection, supercube, distance, cofactor, Sharp. Disjoint Sharp, Consensus, Computation of all prime implicants.	Chapter 7
9	U 1/11	Computation of all prime implicants, Tautology, Containment. Complementation.	Chapter 7
10	T 3/11	**Exact two-level minimization**, ESPRSSSO-EXACT. **Heuristic minimization**, Heuristic minimization operators: Expand, Reduce, Irredundant, Reshape. Expand heuristics.	Chapter 7

11	U 8/11	Expand heuristics, Reduce.	Chapter 7
	M 9/11	**Major Exam I**	
12	T 10/11	Reduce, Irredundant, Essentials. Espresso Algorithm.	Chapter 7
	W 11/11	**Last day dropping with W**	
13	U 15/11	No Class.	
14	T 17/11	Testability of Two Level circuits. Logic Network, Network optimization, Area Estimation. **Mutlilevel transformations**: Elimination, Decomposition, Factoring.	Chapter 7 & 8
	21/11-2/12	**E i d A d h a H o l i d ay**	
15	U 6/12	**Mutlilevel transformations**: Extraction, Simplification, Substitution. Elimination algorithm. **Algebraic model**. Algebraic division algorithm.	Chapter 8
	M 7/12	Substitution algorithm, Extraction, Kernels, Kernels computation. **Kernel Set Computation**, Recursive Kernel Computation, Matrix Representation of Kernels. Single-Cube Extraction, Multiple-cube extraction.	Chapter 8
16	T 8/12	Value of a Kernel. **Decomposition**. **Factorization** Algorithm: quick & Good Factoring. **Fast Extraction** Algorithm: Double-cube divisors and single-cube divisors.	Chapter 8
17	U 13/12	**Fast Extraction** Algorithm: Double-cube divisors and single-cube divisors, Boolean Methods, Controllability & Observability don't care conditions. **Satisfiability don't care** conditions, Controllability don't care computation. Observability don't care conditions computation.	Chapter 8
	M 14/12 (Makeup)	Multi-Way Stems Theorem, Observability Don't Care Algorithm, Transformations with don't cares. Optimization and perturbations.	Chapter 8
18	T 15/12	Synthesis and testability, **Synthesis for testability**. Timing issues in multilevel logic optimization, **delay modeling**, topological critical path.	Chapter 8
19	U 20/12	No Class.	
20	T 22/12	No Class	
	W 23/12	**Last day dropping all courses with W**	
		1st Paper Presentation	
21	U 27/12	False path problem, Algorithms for delay minimization, Transformations for delay reduction. More refined delay models, Speedup algorithm. **Library Binding**: Library Models.	Chapter 8 & 10
	M 28/12 (Makeup)	**Library Binding**: Major Approaches, Rule-based library binding, Algorithms for library binding, Partitioning, Decomposition, Matching, Covering. Tree-based matching. **Tree-based covering.**	Chapter 10

22	T 29/12	**Minimum Delay Cover**: constant and load-dependent delays, **Boolean matching**: Signatures and Filters.	Chapter 10
23	U 3/1	**Sequential Logic Synthesis**: Modeling Synchronous circuits, **State minimization** for completely and incompletely-specified FSMs.	Chapter 9
24	T 5/1	**State minimization** for incompletely-specified FSMs. **State Assignment**. State encoding for two-level models.	Chapter 9
	Th. 7/1	**Major Exam II**	
25	U 10/1	Symbolic minimization, **Input encoding problem.** Dichotomy theory, Exact & Heuristic input encoding.	Chapter 7 & 9
26	T 12/1	**Output and mixed encoding**, Covering and Disjunctive relation. State encoding for two-level implementation, Synchronous logic network, **Retiming**.	Chapter 7 & 9
27	U 17/1	**Architectural-level synthesis**, Data-flow graphs, **Sequencing graphs**, Behavioral optimization of sequencing graphs. Synthesis in the temporal domain: **Scheduling**, Synthesis in the Spatial domain: **Binding.** Scheduling Models, Minimum latency unconstrained scheduling, ASAP & ALAP scheduling.	Chapter 3 & 4
28	T 19/1	Latency Constrained Scheduling, Scheduling under Resource Constraints, ILP Formulation, List Scheduling Algorithm for Minimum Latency.	Chapter 5
	W 20/1	**Dropping all courses with WP/WF**	
	Th. 21/1	List Scheduling Algorithm for Minimum Resource Usage, Algorithmic Solution to the Optimum Binding Problem, ILP Formulation of Binding, Register Binding Problem. Left-Edge Algorithm	Chapter 5 & 6
29	U 24/1	**2nd Paper Presentations**	
30	T 26/1	**2nd Paper Presentations**	