KING FAHD UNIVERSITY OF PETROLEUM & MINERALS

COMPUTER ENGINEERING DEPARTMENT

COE 561: Digital System Design and Synthesis
Term 061 Lecture Breakdown

	Date	Topics	Ref.
1	U 10/9	Syllabus, Introduction.	Chapter 1
2	T 12/9	**Introduction**: Microelectronics Design Problems, Microelectronics Design Styles.	Chapter 1
3	U 17/9	Dealing with design complexity, Design domains and levels of abstractions, Digital system design, Design vs. synthesis, Digital system design cycle, Synthesis process.	Chapter 1
4	T 19/9	High-level synthesis, Design and evaluation space, Combinational design space example, Architecture design space example, Pareto Optimality.	Chapter 1
5	U 24/9	**Logic Synthesis Background**: Boolean Algebra, Boolean Functions, Shannon's Theorem.	2.5
6	T26/9	Unate functions, Boolean difference, Consensus, Smoothing, Orthonormal Basis Expansion.	2.5
7	U 1/10	Orthonormal Basis Expansion Representation of Boolean functions, **Binary Decision Diagrams.** Reduced Binary Decision Diagrams	2.5
8	T3/10	Reduced Binary Decision Diagrams, **ITE DAGs**, **Satisfiability**,	2.5
9	U 8/10	**Minimum Covering Problem, Branch & Bound Algorithm**. Covering reduction strategies, Exact Cover.	2.5
10	T 10/10	**Two-level minimization** definitions, PLA minimization, **Positional cube notation**, Operations on logic covers: cofactor, Sharp.	Chapter 7
11	U 29/10	Disjoint Sharp, Consensus, Computation of all prime implicants, Tautology	Chapter 7
12	T 31/10	Tautology, Containment, Complementation. **Exact two-level minimization**, ESPRSSSO-EXACT.	Chapter 7
13	U 5/11	**Heuristic minimization**, Heuristic minimization operators: Expand, Reduce, Irredundant, Reshape.	Chapter 7
14	T 7/11	Expand heuristics. Solution of Major Exam I.	Chapter 7
15	U 12/11	Expand heuristics	Chapter 7
16	T 14/11	Reduce, Irredundant, Essentials. Espresso Algorithm. Testability of Two Level circuits.	Chapter 7
17	U 19/11	No class.	
18	T 21/11	Logic Network, Network optimization, Area Estimation. **Mutlilevel transformations**:	Chapter 8

		Elimination, Decomposition, Factoring, Extraction, Simplification, Substitution. Elimination algorithm	
19	U 26/11	**Algebraic model**, Algebraic division algorithm, Substitution algorithm, Extraction, Kernels, Kernels computation.	Chapter 8
20	T 28/11	**Kernel Set Computation**, Recursive Kernel Computation, Matrix Representation of Kernels, Single-Cube Extraction, Multiple-cube extraction, **Decomposition**. **Factorization** Algorithm: quick & Good Factoring.	Chapter 8
	S 2/12	**Fast Extraction** Algorithm: Double-cube divisors and single-cube divisors, Boolean Methods, Controllability & Observability don't care conditions.	Chapter 8
21	U 3/12	**Satisfiability don't care** conditions, Controllability don't care computation, Observability don't care conditions computation. Transformations with don't cares.	Chapter 8
22	T 5/12	Optimization and perturbations, synthesis and testability, **Synthesis for testability,** timing issues in multilevel logic optimization, **delay modeling**, topological critical path. False path problem, Algorithms for delay minimization, Transformations for delay reduction, More refined delay models, Speedup algorithm.	Chapter 8
23	U10/12	**Library Binding**: Rule-based library binding, Algorithms for library binding, Partitioning, Decomposition, Matching, Covering, Tree-based matching.	Chapter 10
24	T 12/12	**Tree-based covering, Minimum Delay Cover**: constant and load-dependent delays, **Boolean matching**: Signatures and Filters.	Chapter 10
25	U 17/12	**Sequential Logic Synthesis**: Modeling Synchronous circuits, **State minimization** for completely-specified FSMs, **State Assignment**. State encoding for two-level models. Symbolic minimization, **Input encoding problem.**	Chapter 7 & 9
26	T 19/12	Dichotomy theory, Exact & Heuristic input encoding. **Output and mixed encoding**, Covering and Disjunctive relation.	Chapter 7 & 9
27	U 7/1	**Output and mixed encoding**, State encoding for two-level implementation, Synchronous logic network, **Retiming**.	Chapter 7 & 9
28	T 9/1	**Architectural-level synthesis**, Data-flow graphs, **Sequencing graphs**, Behavioral optimization of sequencing graphs. Synthesis in the temporal domain: **Scheduling**, Synthesis in the Spatial domain: **Binding**, Approached to Architectural	Chapter 3 & 4

		Optimization	
	S 13/1 (Makeup)	Scheduling Models, Minimum latency unconstrained scheduling, **ASAP & ALAP** scheduling, Latency Constrained Scheduling, Scheduling Under detailed timing constraints: minimum and maximum timing constraints. Scheduling under Resource Constraints, **ILP Formulation**.	Chapter 5
29	U 14/1	**ILP Formulation**. **List scheduling** for minimum latency under resource constraints. List Scheduling Algorithm for Minimum Resource Usage. Scheduling graphs with alternative paths.	Chapter 5
30	T 16/1		