COE 561, Term 081

Digital System Design and Synthesis

Project Selection

Project No.	Project Title	Members
1	**Enhancing Design Robustness with Reliability-aware Resynthesis and Logic Simulation**	ZAID ZURAIGAT TAMEEM AL-MANI
2	**Reliability-Driven Don't Care Assignment for Multi-Level Logic Synthesis**	Mohammed Asif Irfan Khan
3	**Reliability-Driven State Assignment for Sequential Logic Synthesis**	Abdulaziz Tabakh Ayed Al-Qahtani
3	**Reliability-Driven State Assignment for Sequential Logic Synthesis**	Ahmad AlRefai Wael Al Takrouri
4	**Implementation of ITE DAG**	Orwa Diraneyya Isah Lawal
5	**Heuristic-Based Two-Level Logic Minimization Based on Covering**	MAHER KAMAL AHMAD ALI