Name: **Id#**

COE 405, Term 181

Design & Modeling of Digital Systems

Quiz# 5

Date: Sunday, Nov. 25, 2018

Q.1. It is required to write a parametrizable Verilog module to model a Queue data structure (First In First Out) with N elements each with M bits. The Queue has M-bit DataOut signal which outputs the content of the Queue when the Queue is read by setting signal Read=1. It also has M-bit DataIn signal which holds the value to be written to the Queue by setting signal Write=1. The Queue has also three additional output signals: Empty to indicate that the Queue is empty, Full to indicate that the queue is full and Error. The Error signal is set when the Queue is requested to be read while it is empty or when the Queue is requested to be written while it is full. In the case of Error, no action will be done by the Queue. Assume also that when both Read and Write signals are set, the Queue will neither be read nor written. Assume that the Queue has synchronous reset which will reset the Queue to the empty state when asserted. Complete the given Verilog module which uses a counter to keep track of whether the queue is full or empty.

```
module Queue #(parameter N=4, M=4)(output reg [M-1:0] DataOut,
output Full, Empty, Error,  input [M-1:0] DataIn, input Read,
Write, Reset, CLK);

reg [log2(N):0] CNT;
reg [log2(N)-1:0] First, Last;
reg [M-1:0] Queue [N-1:0];


assign Error =
assign Empty =
assign Full  =
```

```
function integer log2 (input integer n);
      integer i;
      begin
  log2 = 1;
  for (i=0; 2**i<n; i=i+1)
       log2 = i+1;
       end
endfunction


endmodule
```