Name: **Id#**

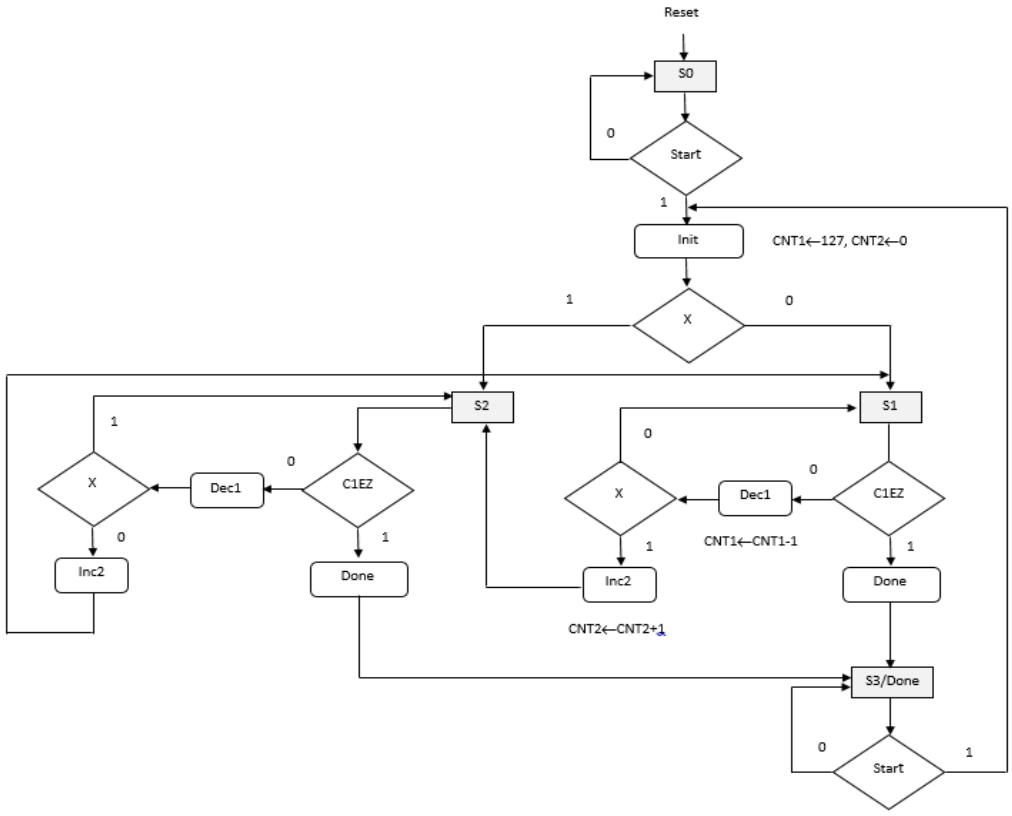
COE 405, Term 152

Design & Modeling of Digital Systems

Quiz# 5

Date: Sunday, April 24, 2016

Q.1. It is required to design a circuit that counts the number of data transitions (i.e. 0→1and 1→0 data changes) through a stream of 128 bit data. The data is applied serially through an input *X* once the user presses a *Start* button, where the first bit is transmitted in the same cycle the *Start* button is asserted. Once the computation is finished the machine asserts a *Done* signal which remains asserted until the user presses the Start button again or resets the machine. Assume that the machine has Asynchronous *Reset* input. The ASMD chart for this machine is given below.



(i) Write a behavioral Verilog module to model the data path unit for the given ASMD chart for circuit.

(ii) Write a behavioral Verilog module to model the control unit for the given ASMD chart for this circuit.

(iii) Write a Verilog module to model the overall circuit by connecting the data path and control unit modules.