Name: **Id#**

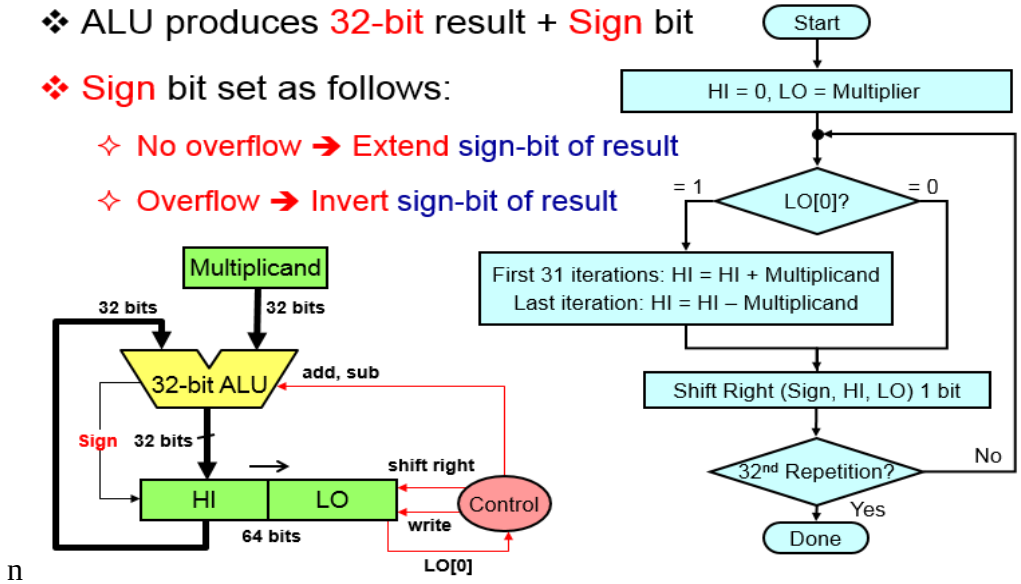
COE 405, Term 162

Design & Modeling of Digital Systems

Quiz# 4 Solution

Date: Tuesday, May 1, 2017

Q1. It is required to design an **n-bit signed multiplier** circuit. The architecture and the algorithm for performing signed multiplication are given below:



n

Write a parametrizable Verilog module to model the signed multiplication circuit as a combinational circuit using for loop.

```
module MULC #(parameter N=4) (output reg [N-1:0] HI, LO, input [N-1:0] A, B);
integer i;
reg [N-1:0] C;
reg OVF, Sign;
always @(A, B) begin
  HI = 0;  LO = B;
  for (i=0; i<N; i=i+1) begin
     if( LO[0] ) begin
        if ( i==N-1 ) begin
             C = HI - A;
             OVF = (HI[N-1] ^ A[N-1]) & (HI[N-1]^C[N-1]);
        end
        else begin
            C = HI + A;
            OVF = (HI[N-1] ~^ A[N-1]) & (HI[N-1]^C[N-1]);
        end
        Sign = OVF ^ C[N-1];
        HI = C;
     end
     else Sign = HI[N-1];
   {HI, LO} = {Sign, HI,  LO[N-1:1]};
  end
end
endmodule
```