Name: **Id#**

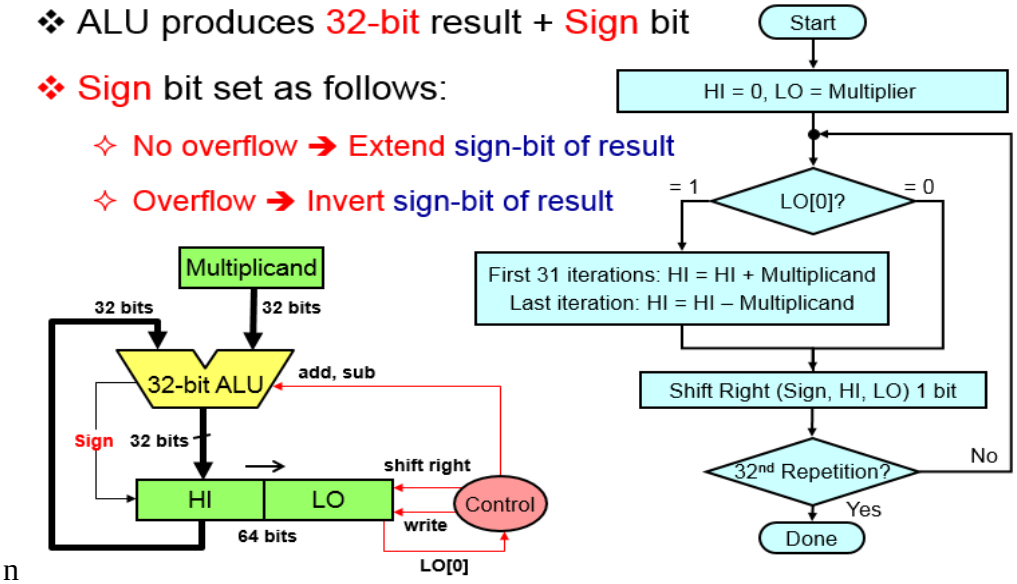
COE 405, Term 162

Design & Modeling of Digital Systems

Quiz# 4

Date: Tuesday, May 1, 2017

Q1. It is required to design an **n-bit signed multiplier** circuit. The architecture and the algorithm for performing signed multiplication are given below:



n

Write a parametrizable Verilog module to model the signed multiplication circuit as a combinational circuit using for loop.