Name: **Id#**

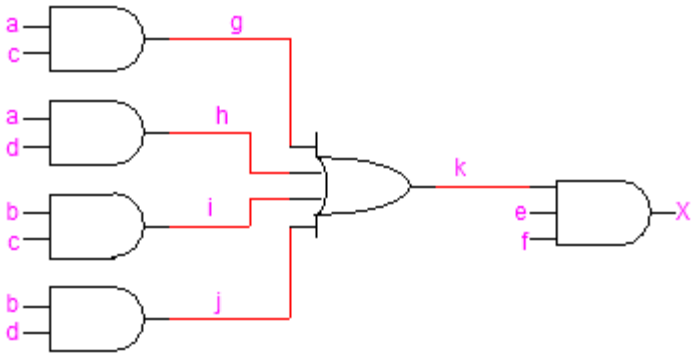
COE 405, Term 122

Design & Modeling of Digital Systems

Quiz# 4

Date: Monday, April 29, 2013

Q.1. Consider the logic network below with inputs *{a, b, c, d, e, f}* and output *{X}*:



Assume that the delay of a gate is related to the number of its inputs i.e. the delay of a 2-input AND gate is 2. Also, assume that the input data-ready times are zero for all inputs except input *a*, which has a data-ready time of 2.

(i) Compute the data ready times and slacks for all vertices in the network.

(ii) Determine the topological critical path.

(iii) Suggest an implementation of the function *X* to reduce the delay of the circuit to the minimum possible and determine the maximum propagation delay in the optimized circuit. Has the area been affected?

Q.2. Determine possible circuits that will be synthesize by each of the following modules:

(i)
```
module m1  (output y, input e1, e2, x1, x2);
        assign y = e1?x1:e2?x2:y;
endmodule
```

(ii)
```
module m2  (output y, input e1, e2, x1, x2);
        assign y = e1?x1:e2?x2:1'bx;
endmodule
```

(iii)
```
module m3 #(parameter size=2)(
output  reg y,
input [size-1:0] a, b );
integer k;
always @ (a, b) begin
  for (k=size-1; k>=0; k=k-1) begin
      if (a[k] != b[k])
         y = 0;
  end
end
endmodule
```

(iv)
```
module m4 #(parameter size=3)(
    output  reg y,
    input [size-1:0] x );
    always @ (x) begin
              y = 0;
             if (x[0]) y=1;
             else if (x[1]) y=1;
             else if (x[2]) y=1;
    end
    endmodule
```

(v)
```
module m5 #(parameter size=3)(
    output  reg y,
    input [size-1:0] x );
    integer k;
    always @ (x) begin
      y = 1;
      for (k=1; k<size; k=k+1)
            y = y & x[k];
      if (!x[0]) y = 1'bz;
    end
    endmodule
```

(vi)
```
module m6 (
    output  reg y,
    input x1, x2, x3);
    always @ (x1, x2, x3) begin
      if (x1) y = x2 ^ x3;
    end
    endmodule
```