Name: **Id#**

COE 405, Term 181

Design & Modeling of Digital Systems

Quiz# 3 Solution

Date: Thursday, October 18, 2018

Q.1. Consider the given FSM that has 7 states, one input (X) and one output (Z), represented by the following state table:

Present State	Next State		Output (Z)	
	X=0	X=1	X=0	X=1
S0	S1	S2	1	0
S1	S3	S4	1	1
S2	S4	S6	0	0
S3	S5	S4	0	0
S4	S5	S1	1	1
S5	S3	S4	0	0
S6	S1	S2	0	0

(i) Determine the equivalent states.

Using Partition Refinement Method:
P1 = {(s0), (s1, s4), (s2, s3, s5, s6)}
P2 = {(s0), (s1, s4), (s2, s6), (s3, s5)}
P3 = {(s0), (s1, s4), (s2, s6), (s3, s5)}

Thus, the equivalent states are:

- States s1 and s4
- States s2 and s6
- States s3, and s5

(ii) Reduce the state table into minimum number of states and show the reduced state table.

Present State	Next State		Output (Z)	
	X=0	X=1	X=0	X=1
S0	S1	S2	1	0
S1	S3	S1	1	1
S2	S1	S2	0	0
S3	S3	S1	0	0

Q.2. It is required to design a sequential circuit using Mealy model that computes the equation Z=3*X-2*Y, where X and Y are unsigned numbers that will be fed serially. Assume that the circuit has an asynchronous Reset input that resets the machine to the reset state. Draw the state diagram for your sequential circuit. Make sure that your state machine is minimal and that it does not have any redundant state.