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COE 405, Term 162

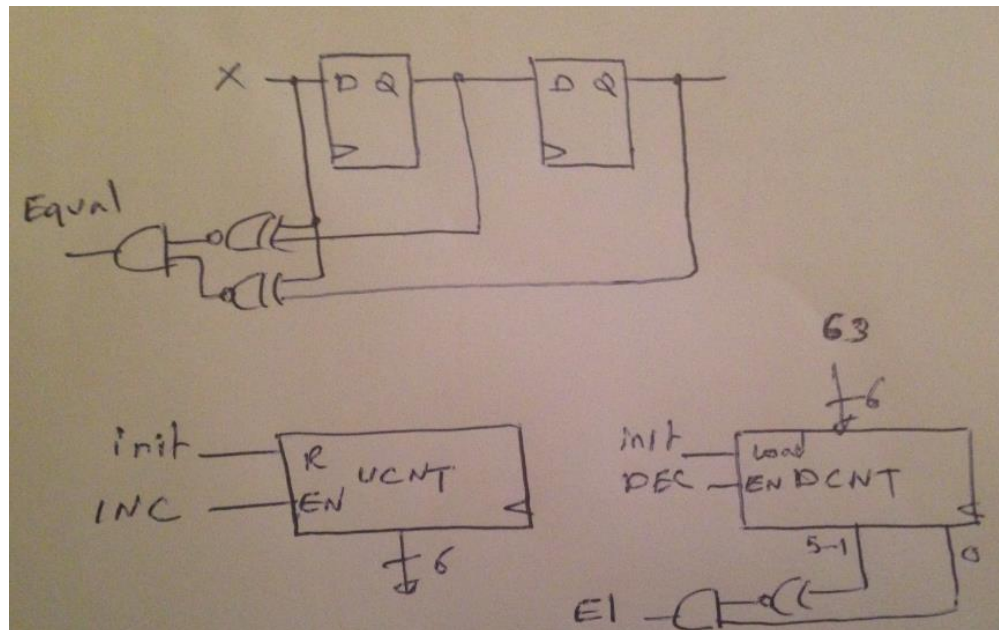
Design & Modeling of Digital Systems

Quiz# 3 Solution

Date: Thursday, April 13, 2017

Q.1. It is required to design a circuit that counts the number of 3-equal consecutive bits (i.e. 000 or 111) through a stream of 64 bit data. The data is applied serially through an input X once the user presses a *Start* button, where the first bit is transmitted in the same cycle the *Start* button is asserted. Once the computation is finished the machine asserts a *Done* signal which remains asserted until the user presses the *Start* button again or resets the machine. Assume that the machine has Asynchronous *Reset* input.

- (i) Show the Data path components needed for designing this circuit along with their control signals.



(ii) Show the ASMD chart for control unit of the circuit.

