Name: KEY **Id#**

COE 405, Term 152

Design & Modeling of Digital Systems

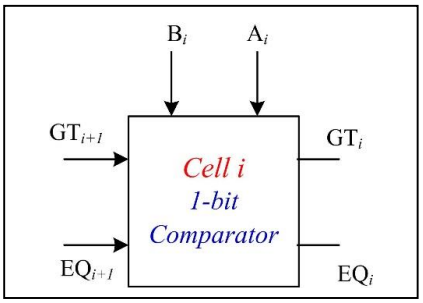
Quiz# 3

Date: Sunday, April 3, 2016

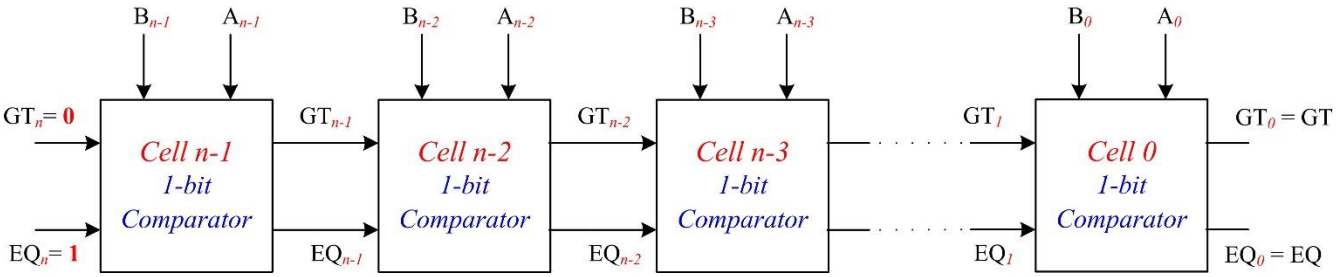
Q1. Given below the design of an *n*-bit magnitude comparator. The circuit receives two *n*-bit unsigned numbers ***A*** *and* ***B*** and produces two outputs **GT** and **EQ** as given in the table to the right.

	GT	EQ
IF A > B	1	0
IF A = B	0	1
IF A < B	0	0

The input operands are processed in a bitwise manner *starting with the most significant bit (MSB)*. The comparator circuit is constructed using *n identical copies* of the basic 1-bit *cell* shown to the right.



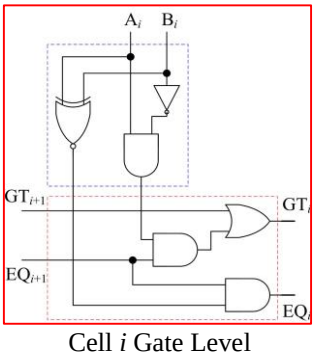
The Figure below shows the *n*-bit comparator circuit implemented using *n* copies of the basic 1-bit cell.



Boolean expressions of the outputs of ***cell i*** and its gate-level implementation are given below:

$$GT_i = GT_{i+1} + A_i \, \bar{B}_i \, EQ_{i+1}$$
$$EQ_i = (A_i \odot B_i).\, EQ_{i+1}$$

(i) Write a Verilog model **Comp1Bit** to model the 1-bit comparator circuit using *either* a structural model of basic logic gates *or* a behavioral model using the **assign** statement.



Cell *i* Gate Level Implementation

The declaration of the Comp1Bit module is as follows:

```
module Comp1Bit (output GT_out, EQ_out , input GT_in , EQ_in, Ai, Bi);
```

```
module Comp1Bit (output GT_out, EQ_out, input GT_in, EQ_in, Ai, Bi);
        assign GT_out = GT_in || Ai && !Bi && EQ_in;
        assign EQ_out = (Ai ~^ Bi) && EQ_in;
endmodule
```

OR

```
module Comp1Bit (output GT_out, EQ_out, input GT_in, EQ_in, Ai, Bi);
not (g1, Bi);
and (g2, g1, Ai);
xnor(g3, Ai, Bi);
and (g4, g2, EQ_in);
or  (GT_out, GT_in, g4);
and (EQ_out,  EQ_in, g3);
endmodule
```

(ii) Complete the following Verilog model **Comp3Bit** that models a 3-bit comparator circuit.

```
module Comp3Bit (output Greater, Equal,
                        input [2:0] A , B) ;

wire  [2:1]  GT, EQ ; // internal wires connecting cells
/* First instance "M1" of the cell Comp1Bit with its inputs GT_in and  EQ_in
connected to fixed values of 0 and 1 respectively */
//
Comp1Bit M1 (GT[2] , EQ [2], 1'b0, 1'b1, A[2], B[2]);
Comp1Bit M2 (GT[1], EQ[1], GT[2], EQ[2], A[1], B[1]);
Comp1Bit M3 (Greater, Equal, GT[1], EQ[1], A[0], B[0]);
endmodule
```

(iii) Write a Verilog test bench to test the 3-bit comparator **Comp3Bit** by applying the following input patterns consecutively with a delay of 20ps:

1. {A=100, B=011},
2. {A=101, B=101},
3. {A=011, B=111}.

```
module t_Comp3Bit();
  wire     Greater, Equal;
  reg      [2:0] A, B;
  Comp3Bit M1 (Greater, Equal, A, B) ;

initial begin
    A=3'b100; B=3'b011;
    #20 A=3'b101; B=3'b101;
    #20 A=3'b011; B=3'b111;
  end
endmodule
```