Name: **Id#**

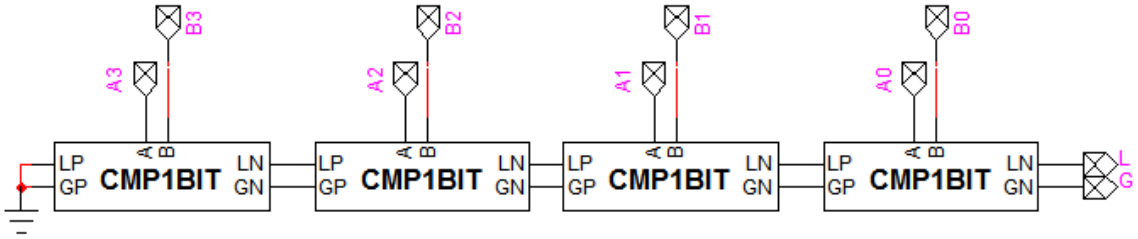
COE 405, Term 131

Design & Modeling of Digital Systems

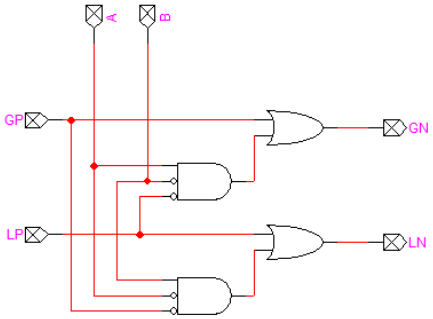
Quiz# 3

Date: Thursday, Nov. 28, 2013

Q.1. It is required to model an n-bit iterative magnitude comparator. A 4-bit comparator is shown below:



The model for a 1-bit comparator is as follows:



Write a parametrizable Verilog model for modeling an n-bit comparator with a default of n=4.

Q.2. The ASMD chart given below describes a state machine that counts 1's in a word and terminates activity as soon as possible. The machine remains in its reset state, *S_idle*, until an external agent asserts *start*. This action asserts the output, *load_temp*, which will cause *data* to be loaded into register *temp* when the state makes a transition to *S_counting* at the next active edge of *clk*. The machine remains in *S_counting* while *temp* contains a 1. Two actions occur concurrently at each subsequent clock: (1) *temp* is shifted towards its LSB and (2) *temp[0]* is added to *bit_count*. When *temp* finally has a 1 in only the LSB, the machine's state moves to *S_waiting*, where *done* is asserted. The state remains in *S_waiting* until *start* is reasserted. Assume that when the synchrnous *reset* input is asserted the machine is reset to the state *S_idle* and *bit_count* and *temp* are initialized to 0.

(i) Write a Verilog model for modeling the data-path unit.

(ii) Write a Verilog model for modeling the control unit using the following state assignment: *S_idle=00, S_counting =01*, and *S_waiting=10*.