Name: **Id#**

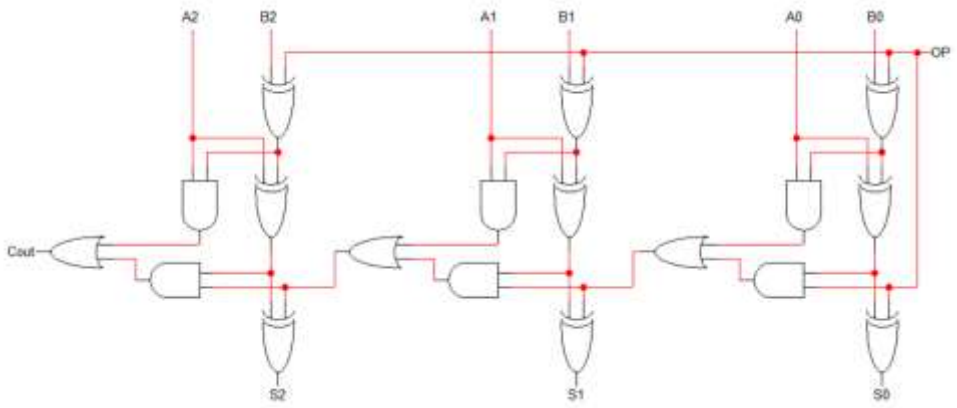
COE 405, Term 181

Design & Modeling of Digital Systems

Quiz# 2 Solution

Date: Sunday, October 7, 2018

Q.1. The circuit given below is a 3-bit adder/subtractor. The circuit performs addition when OP=0 and performs subtraction otherwise.



(i) Write a Verilog model to model a 1-bit cell design of the circuit using either primitive gates or assign statement.

```
module addsubcell (output cout, sum, input a, b, cin, op);

assign op2 = b ^ op;
assign p = a ^ op2;
assign g = a & op2;
assign sum = p ^ cin;
assign cout = g | p & cin;

endmodule
```

(ii) Write a parametrizable Verilog model for modeling an n-bit adder/subtractor circuit using generate loop construct.

```
module addsub #( parameter n = 3)
(output cout, output [n-1:0] sum,
 input  [n-1:0] a, b, input op);
```

```
wire [n:0] carry;

assign carry[0] = op;
assign cout = carry[n];
genvar i;

for ( i = 0; i < n; i = i+1 ) begin : ripple
   addsubcell AS(carry[i+1], sum[i], a[i], b[i], carry[i], op);
end

endmodule
```

(iii) Write a test bench that instantiates and tests a 3-bit adder/subtractor circuit by applying the following input patterns to your circuit with a delay of 30 unit delays between successive input patterns: {(A=1, B=5, OP=0), {(A=1, B=5, OP=1), (A=7, B=7, OP=0), (A=0, B=7, OP=1)}.

```
module t_addsub();
 wire       [2:0] sum;
 reg        [2:0] a, b;
 reg   op;

 addsub M1 (cout, sum, a, b, op);

initial begin
    a=3'b001; b=3'b101; op=1'b0;
   #30      op=1;
   #30      a=3'b111; b=3'b111; op=1'b0;
   #30      a=3'b000; b=3'b111; op=1'b1;

 end
endmodule
```