Name: Key **Id#**

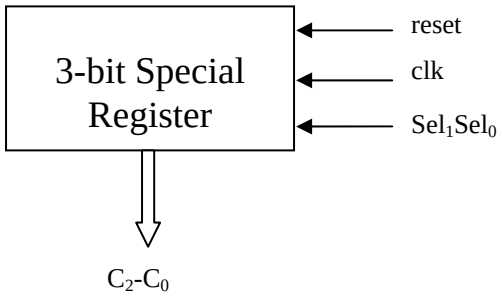
COE 405, Term 021

Design & Modeling of Digital Systems

Quiz# 2

Date: Monday, October 21, 2002

Q.1. It is required to design a 3-bit register that has the capability to count up, count down, shift left logically, or shift right logically based on a 2-input select. The interface description of the 3-bit register is shown below, where **sel** determines the operation. When sel=00, the register will count up, when sel=01, it will count down, when sel=10, it will shift left logically, and when sel =11, it will shift right logically. The reset is a synchronous reset and the register is rising-edge triggered.



(i) Describe an Entity **CS3** for the 3-bit register using type BIT and BIT_VECTOR for the interface signals.

```
Entity CS3 IS
   PORT (reset, clk: IN BIT; sel: IN BIT_VECTOR(1 downto 0); C: OUT
   Bit_Vector(2 Downto 0));
   Constant limit: INTEGER :=7;
END CS3 ;
```

(ii) Model a behavioral Architecture **Behave** for this 3-bit register.

```
Architecture Behave OF CS3 IS
Begin
   Process(clk)
          Variable count: INTEGER := 0;
   Begin
      IF (clk = '1' AND clk'Event ) THEN
            IF reset = '1' THEN  count := 0;
            ELSE
              CASE sel is
                   when "00" => count := count+1;
                   when "01" => count := count-1;
                   when "10" => count := count*2;
                   when "11" => count := count/2;
              END case;
            END IF;
            IF (count > limit) Then count := count-limit-1;
            ELSE IF count= -1 Then count := limit; END IF;
            END IF;
      END IF;
      Case count is
            when 0 => c <= "000";
            when 1 => c <= "001";
            when 2 => c <= "010";
            when 3 => c <= "011";
            when 4 => c <= "100";
            when 5 => c <= "101";
            when 6 => c <= "110";
            when 7 => c <= "111";
            when others => c <= "000";
      End Case;
     END process;
END Behave ;
```