Name: **Id#**

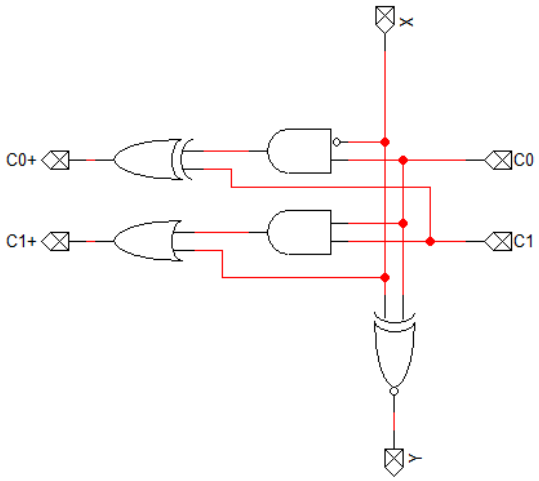
COE 405, Term 162

Design & Modeling of Digital Systems

Quiz# 2

Date: Tuesday, March 14, 2017

Q.1. Consider the combinational circuit given below modeling a 1-bit cell for computing the equation Y=3*X-1, which has three inputs C1, C0, and X and three outputs C1+, C0+ and Y:



(i) Write a Verilog model to model the 1-bit cell design of the circuit using either primitive gates or assign statement.

(ii) Write a Verilog model for modeling a 3-bit circuit for computing the equation Y=3*X-1 by instantiating three copies of this cell and connecting C1 and C0 of the first cell to 00, C1+ and C0+ of the first cell to C1 and C0 of the 2nd cell, C1+ and C0+ of the 2nd cell to C1 and C0 of the 3rd cell.

(iii) Write a test bench that tests your 3-bit circuit by applying the following input patterns to your cell (X2X1X0)={000, 001, 010, 111} and observing the obtained outputs Y2Y1Y0.

Q.2. It is required to design a sequential circuit using Mealy model that computes the equation Y=X-3, where X is an unsigned number that will be fed serially. Assume that the circuit has an asynchronous Reset input that resets the machine to the reset state. Draw the state diagram or state table for your sequential circuit. Make sure that your state machine is minimal and that it does not have any redundant state.