Name: **Id#**

COE 405, Term 152

Design & Modeling of Digital Systems

Quiz# 2

Date: Sunday, Feb. 28, 2016

Q.1.   It is required to design a sequential circuit that has a single input X representing a signed 2's complement number and a single output Y. The circuit receives the number serially through the input X from the least significant bit (LSB) to the most significant bit (MSB), and computes the equation Y=X-3 and generates the output serially from the least significant bit to the most significant bit. The circuit has an additional asynchronous reset input R that resets the circuit into an initial state. The following are examples of input and output data:

Examples:

		LSB				MSB	
Input	X	0	1	1	0	0	Input=6
Output	Y	1	1	0	0	0	Output=3

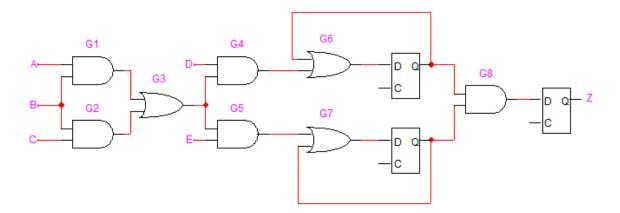|		LSB				MSB	
Input	X	0	0	1	1	0	Input=12
Output	Y	1	0	0	1	0	Output=9

Draw a state diagram or show the state table of the circuit with minimum number of states assuming a **Mealy** model. You are not required to implement the circuit.

Q.2. Consider the given FSM that has 4states, one input X and one output Z, represented by the following state table:

Present State	Next State, Z	
	X=0	**X=1**
S0	S1, 0	S2, 0
S1	S0, 0	S3, 0
S2	S2, 0	S3, 1
S3	S3, 0	S2, 1

(i) Determine the equivalent states.

(ii) Reduce the state table into the minimum number of states and show the reduced state table.

Q.3. Consider the sequential circuit given below having 5 inputs {A, B, C, D, E} and one output {Z}. Assume that the delay of a gate is related to the number of inputs i.e. the delay of a 2-input AND gate is 2 unit delays and the delay of a 2-input OR gate is 2 unit delays.

(i) Determine the critical path of this circuit and the maximum propagation delay.

(ii) Using only the **Retiming** transformation, reduce the critical path of this circuit with the minimum number of flip-flops possible. Determine the maximum propagation delay after retiming.