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COE 405, Term 162

Design & Modeling of Digital Systems

Quiz#1 Solution

Date: Tuesday, Feb. 28, 2017

Q.1. One of the design optimization criteria is the area of the design. Discuss why area optimization is important. List two other design optimization criteria and discuss how they can be optimized.

Area is optimized to reduce the manufacturing and packaging cost and also to improve the yield.

Other optimization parameters include speed and power.

Speed is optimized by reducing the delay of gates along critical paths.

Power is optimized by reducing the switching probability of gates, using lower VDD, using lower frequency and also by reducing the area of the design.

- **Q.2.** Consider the function: $F(A, B, C) = (A \oplus B) + (A \oplus C)$
 - (i) Compute the expansion of F using the **Orthonormal Basis** $\{\emptyset_1 = \overline{AB}, \emptyset_2 = \overline{AB}, \emptyset_3 = A\overline{B}, \emptyset_4 = AB \}$.

$$F_{A'B'}=C;$$
 $F_{A'B}=1;$ $F_{AB'}=1;$ $F_{AB}=C'$ $F=A'B'(C)+A'B(1)+AB'(1)+AB(C')$

(ii) Compute the function \overline{F} utilizing the orthonormal based expansion of the function.

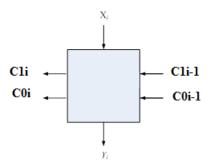
$$F' = A'B' (C') + A'B (0) + AB' (0) + AB (C)$$

= A'B'C' + ABC

- **Q.3.** It is required to design a combinational circuit that computes the equation Y=X-3, where X is an n-bit signed 2's complement number.
 - (i) Design the circuit as a modular iterative circuit where each module receives a single bit of the input, X_i .

The circuit will be design by adding the number $X3\ X2\ X1\ X0 + 1111 + 1111 + 1111$.

This is because -1 is represented in 2's complement as 1111 and -3=-1+-1+-1. Thus, the interface signals between each cell will be carry information which include carry=0, carry=1, carry=2 and carry=3. Thus, we need 2 bits to represent the carry information flow between cells.



(ii) Derive the truth table of your 1-bit module in (i).

C1 _{i-1}	$C0_{i-1}$	Xi	C1 _i	C0 _i	Yi
0	0	0	0	1	1
0	0	1	1	0	0
0	1	0	1	0	0
0	1	1	1	0	1
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	0
1	1	1	1	1	1