Name: KEY **Id#**

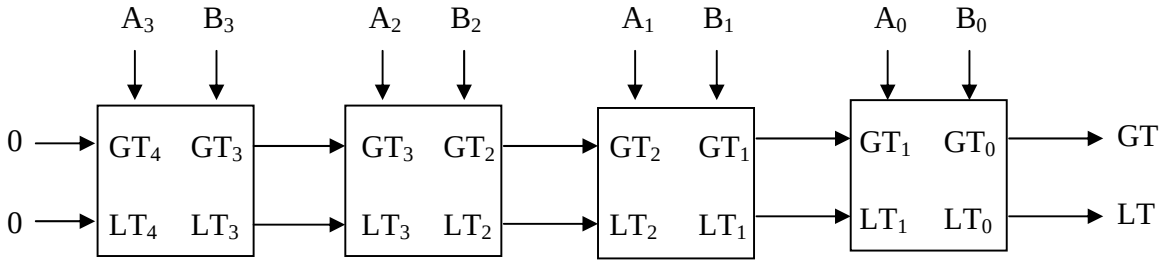
COE 405, Term 062

Design & Modeling of Digital Systems

Quiz# 1

Date: Saturday, March 17, 2007

Q.1. It is required to model a 4-bit comparator that compares two 4-bit numbers $A=A_3A_2A_1A_0$ and $B=B_3B_2B_1B_0$, and produces two outputs GT and LT. If A>B, then the output signal GT is set to 1 and LT is set to 0. If A<B, then the output signal LT is set to 1, and GT is set to 0. Otherwise both signals will be set to 0, which indicates that the two numbers are equal (i.e. A=B). The 4-bit comparator circuit can be designed in a modular way as shown below:



The equations for the 1-bit magnitude comparator can be found to be:

$$GT_i = GT_{i+1} + \overline{LT_{i+1}} A_i \overline{B_i}$$
$$LT_i = LT_{i+1} + \overline{GT_{i+1}} \overline{A_i} B_i$$

(i) Describe an Entity **COMP** for a 1-bit magnitude comparator.

(ii) Model an Architecture **Conc** for this 1-bit COMP using concurrent statements.

(iii) Describe an Entity **COMP4** for a 4-bit magnitude comparator.

(iv) Model Architecture **Struct** for the 4-bit magnitude comparator (**COMP4**) using instantiations of the Entity **COMP**.

(i)
```
Entity COMP is
        PORT (GT, LT, A, B: IN Bit; GTO, LTO: OUT Bit);
end COMP;
```

(ii)
```
Architecture Conc of COMP is
Begin
        LTO <= LT OR (NOT GT AND NOT A AND B);
        GTO <= GT OR (NOT LT AND A AND  NOT B);
end conc;
```

(iii)
```
Entity COMP4 is
    PORT (A, B : IN Bit_Vector(3 downto 0); GT, LT: OUT Bit);
end COMP4;
```

(iv)
```
Architecture Struct of COMP4 is
Component COMP
        PORT (GT, LT, A, B: IN Bit; GTO, LTO: OUT Bit);
end component;
Signal GT3, LT3, GT2, LT2, GT1, LT1: BIT;
signal zero: BIT := '0';
Begin
        U1: COMP Port Map (zero, zero, A(3), B(3), GT3, LT3);
        U2: COMP Port Map (GT3, LT3, A(2), B(2), GT2, LT2);
        U3: COMP Port Map (GT2, LT2, A(1), B(1), GT1, LT1);
        U4: COMP Port Map (GT1, LT1, A(0), B(0), GT, LT);
end Struct;
```