

COE 405, Term 152

Design & Modeling of Digital Systems

HW# 6

Due date: Sunday, April 17

- Q.1.** It is required to design a circuit that computes the average, maximum and minimum of a number of scores N (assuming $0 < N \leq 15$), each score with a value in the range $[0, 15]$. Once a user presses a Start button, the number of scores N will be entered. Then, scores will be entered in subsequent clock cycles one score at a time. Once the circuit finishes computation, it will assert a Done signal and will generate the average, maximum and minimum scores. The average will be shown as an integer number resulting from dividing the sum by N with rounding the result to the nearest integer. The Done signal will remain asserted unless the user presses a Reset button.
- (i) Develop an ASMD chart for the circuit.
 - (ii) Show the design of your data path unit. Write a Verilog module to model your data path.
 - (iii) Write a Behavioral Verilog module to model the ASMD chart of your circuit.
 - (iv) Write a test bench to verify the correct functionality of your circuit. Show snapshots of your simulation to demonstrate its correctness.
 - (v) Implement your circuit on FPGA and demonstrate its correct functionality. Include a link for a video snapshot to demonstrate correct functionality of your circuit on FPGA.

*This assignment can be solved based on a group of two students. The solution should be well organized. Submit a soft copy of your solution in a zip file including your Verilog models. Your solution should be submitted in a **word file** that contains the following items:*

- i. Your name and ID*
- ii. Assignment number*
- iii. Problem statement*
- iv. Your solution*
- v. Include snapshots of simulation output to illustrate the correctness of your models.*