COE 405, Term 031

Design & Modeling of Digital Systems

HW# 6

Due date: Sunday, Jan. 5, 2004

Q.1. It is required to model an n-bit Booth Multiplier. The 4-bit version of this multiplier was discussed in Sec. 1.3.2. The VHDL Entity description of the n-bit multiplier is given below.

```
Entity multiplier is
        Generic (n: integer := 4);
        Port(clk: IN std_logic; dataready: IN std_logic; inputbus : IN
        std_logic_vector (2*n-1 downto 0); busy, done: OUT std_logic; result: OUT
        std_logic_vector ( 2*n-1 downto 0));
End multiplier;
```

The circuit receives two n-bit operands when the input *dataready* becomes 1. This causes the multiplication process to begin and the *busy* flag to become active. Using the add-shift method, the multiplier takes one or two clock cycles for each bit of the multiplicand. When the process is completed, *done* becomes 1 for one clock cycle and *busy* returns to 0. The circuit receives two operands from its *inputbus* and produces the result on its 2n-bit *result* output.

(i) Develop a behavioral model of the n-bit Booth Multiplier. Your behavioral description of the circuit should model it at the clock level. That is, the number of clock cycles that the behavioral model takes for multiplication of the two numbers should be the same as that of the actual circuit using the add-shift method. Verify the correct functionality of your model by simulation of a 4-bit multiplier.

(ii) Develop a dataflow model of the n-bit Booth Multiplier. Divide your multiplier into a data-path and control unit and model each one separately using dataflow modeling style. Verify the correct functionality of your model by simulation by simulation of a 4-bit multiplier..