COE 405, Term 021

Design & Modeling of Digital Systems

HW# 6

Due date: Saturday, Jan. 11, 2003

Q.1. It is required to model in VHDL an arithmetic and logic unit (ALU) with inputs A and B and output C, that can perform any of the following functions shown below based on the three selection lines AS2, AS2, and AS0:

AS2 AS1 AS0	Operation
000	C=A+B
001	C=A-B
010	C=A+1
011	C=A-1
100	C=B
101	C=**NOT** A
110	C= A **AND** B
111	C= A **OR** B

Assume that all the inputs and outputs are of type std_logic. Model the ALU to be of generic size such that the size of the ALU is specified by a generic map.

(i) Simulate a 4-bit ALU to verify the correctness of your model and include simulation sresults.

(ii) Synthesize a 2-bit ALU using Xilinx FPGA tools and demonstrate the functionality of your design.

Q.2. Write a VHDL description for a CMOS memory element with read/write control, enable, and a shared input-output line. When enabled and *rw = 1*, the output is driven by the memory. When enabled and *rw = 0*, the input will be written into the memory. Use qit type.

(i) Using this memory element, write a structural VHDL description for modeling a $\mathbf{2^n}$ **x m** bit memory array ($\mathbf{2^n}$ rows and **m** columns) that has **n** bit address size and **m** bit data size. All input-output lines in a column are wired. The address and data sizes should be generic. Use an n x 2^n row decoder for decoding the address.

(ii) Simulate a $\mathbf{2^3}$ **x 4** (i.e. 8 x 4 with 4-bit address) memory and verify its correct functionality by writing and reading from all addresses.

(iii) Synthesize a $\mathbf{2^3}$ **x 4** (i.e. 8 x 4 with 4-bit address) memory and verify its correct functionality using Xilinx FPGA tools. (**1% Bonus**).