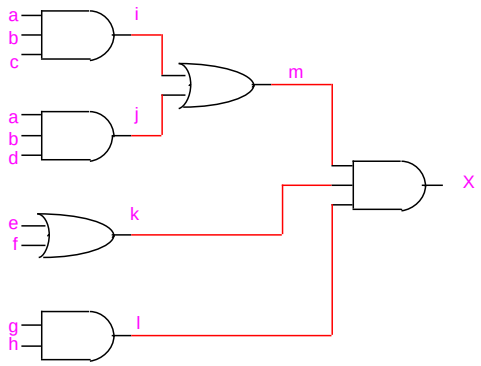
COE 405, Term 131

Design & Modeling of Digital Systems

HW# 5

Due date: Sunday, Dec. 8

Q.1. Consider the logic network below with inputs *{a, b, c, d, e, f, g, h}* and output *{X}*:



Assume that the delay of a gate is related to the number of its inputs i.e. the delay of a 2-input AND gate is 2. Also, assume that the input data-ready times are zero for all inputs.

(i) Compute the data ready times and slacks for all vertices in the network.

(ii) Determine the topological critical path(s).

(iii) Suggest an implementation of the function *X* to reduce the delay of the circuit to the minimum possible and determine the maximum propagation delay in the optimized circuit. Has the area been affected?

Q.2. It is required to design a circuit to compute the equation Y=A+B+C+D+E+F using only two adders. Assume that the inputs will hold their values until the end of the operation. Also, assume that the inputs will be ready when a Start input is asserted and a Done signal will be set when the result is ready.

(i) Show a schedule with minimum latency (i.e., clock cycles) satisfying the area constraints.

(ii) Show the DataPath design of your circuit.

(iii) Show the ASMD diagram of your control unit.

(iv) Model the DataPath and Control units in Verilog and verify the correctness of your model.