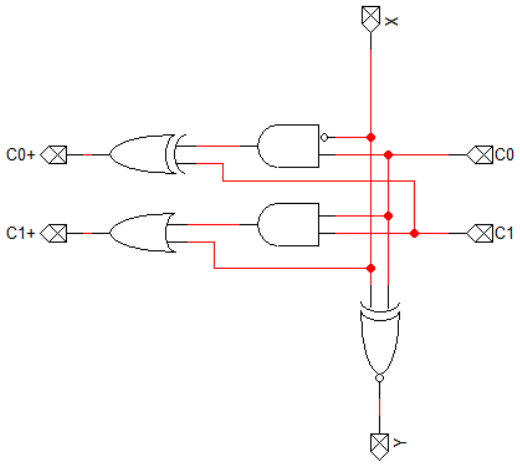
COE 405, Term 152

Design & Modeling of Digital Systems

HW# 4 Solution

Due date: Tuesday, March 22

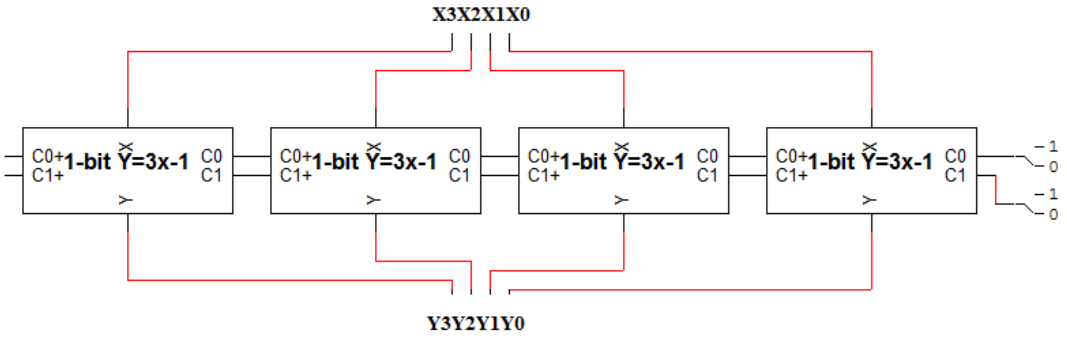
Q.1. An iterative design of a combinational circuit that computes the equation Y=3*X-1, where X is an n-bit signed 2's complement number is given below:



(i) Write a Verilog model to model the given 1-bit cell using primitive gates. Model the delay of AND and OR gates as 5ps, while the delay of XOR and XNOR gates as 8 ps.

```
module Cell3x_1 (output y, c1_, c0_, input x, c1, c0);

and  #5 (g1, ~x, c0);
and  #5 (g2, c0, c1);
xor  #8 (c0_, g1, c1);
or   #5 (c1_, g2, x);
xnor #8 (y, x, c0);

endmodule
```

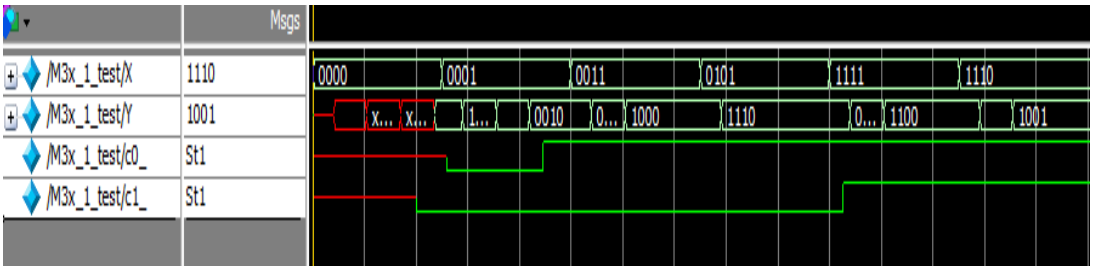
(ii) Write a Verilog model for modeling the circuit given below computing the equation Y=3*X-1 assuming X is a 4-bit number by instantiating 4 cells:




```
module M3x_1 (output c1_, c0_, output [3:0] Y, input [3:0] X);

Cell3x_1 M1 (Y[0], c1_0, c0_0, X[0], 1'b0, 1'b0);
Cell3x_1 M2 (Y[1], c1_1, c0_1, X[1], c1_0, c0_0);
Cell3x_1 M3 (Y[2], c1_2, c0_2, X[2], c1_1, c0_1);
Cell3x_1 M4 (Y[3], c1_, c0_, X[3], c1_2, c0_2);

endmodule
```

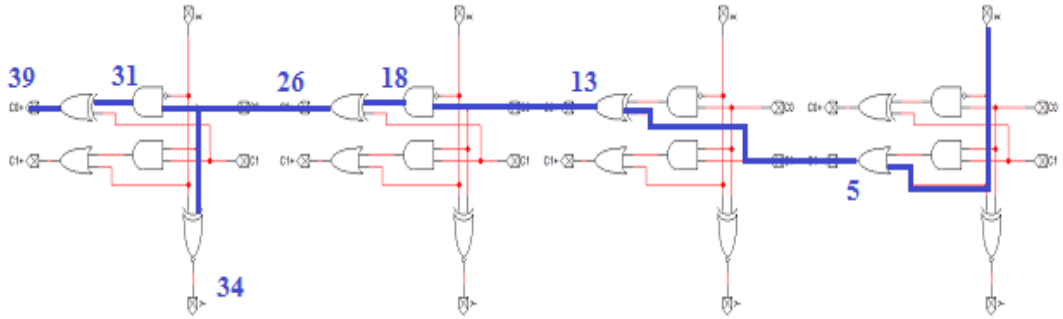
(iii) Write a test bench to test the correctness of your Verilog model by applying the following input patterns $X_3X_2X_1X_0$={0000, 0001, 0011, 0101, 1111, 1110}. Apply consecutive inputs patterns after a delay of 50ps.

```
module M3x_1_test ();
  wire  c1_, c0_;
  wire    [3:0] Y;
  reg   [3:0] X;
  M3x_1 M1 (c1_, c0_, Y, X);


initial begin
    X=4'b0000;
    #50 X=4'b0001;
    #50 X=4'b0011;
    #50 X=4'b0101;
    #50 X=4'b1111;
    #50 X=4'b1110;

  end
endmodule
```



(iv) Determine the longest delay of your 4-bit circuit.

The longest delay is shown in the circuit below, which is 34 if only the y outputs are considered and 39 if the c1+ and c0+ signals are considered.



(v) Write a test bench to verify the longest delay of your 4-bit circuit.

```
module M3x_1_test2 ();
  wire  c1_, c0_;
  wire    [3:0] Y;
  reg   [3:0] X;
  M3x_1 M1 (c1_, c0_, Y, X);


initial begin
    X=4'b0000;
    #50 X=4'b0001;

  end
endmodule
```