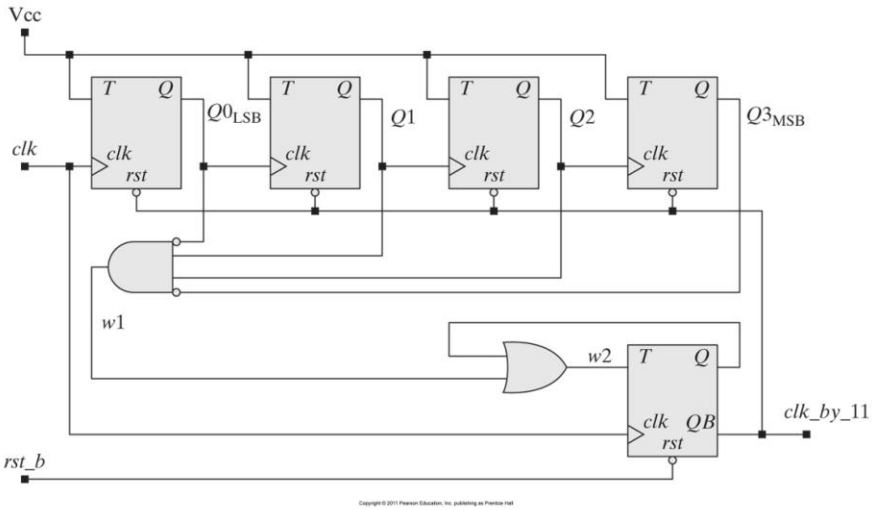
COE 405, Term 122

Design & Modeling of Digital Systems

HW# 4

Due date: Saturday, March 30

Q.1. The schematic shown below is for Divide_by_11, a frequency divider that divides clk by 11 and asserts its output for one clock cycle. The unit consists of a chain of toggle-type flip-flops with additional logic to form an output pulse every 11^{th} pulse of clk. The asynchronous signal rst_b is active-low and drives Q to 1.



(i) Develop a primitive model of a rising-edge triggered T-type flip-flop.

(ii) Develop a structural Verilog model of Divide_ by_11.

(iii) Verify the correctness of your model by using the following test bench:

```
module t_Divide_by_11();
wire clk_by_11;
reg clk, rst_b;
supply1 Vcc;
Divide_by_11 M0 (clk_by_11, clk, rst_b, Vcc);
initial #500 $finish;
initial begin clk = 0; forever #5 clk = ~clk; end
initial begin #10 rst_b = 1; #20 rst_b = 0; #20 rst_b = 1; end

endmodule
```

Q.2. Write a behavioral Verilog model of a rising-edge triggered J-K flip-flop with active-low asynchronous reset. Write a test bench to verify the correctness of your model.

Q.3. Write a behavioral Verilog model of a modulo-6 counter. Assume that the flip-flops are rising-edge triggered and the reset is asynchronous and active high. Write a test bench to verify the correctness of your model.

Q.4. Write a behavioral Verilog model of the data path unit described below. Assume that the flip-flops are rising-edge triggered and the reset is synchronous and active high. Write a test bench to verify the correctness of your model.