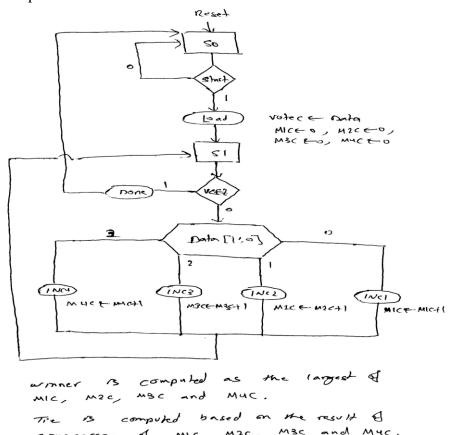
COE 405, Term 131

Design & Modeling of Digital Systems

HW#3 Solution

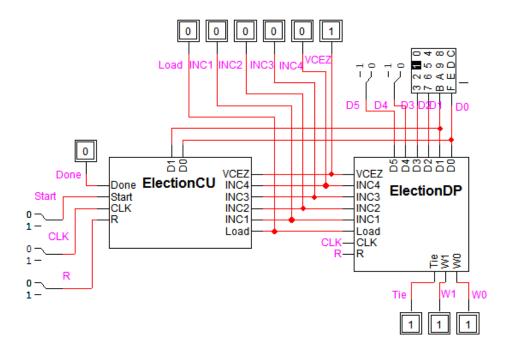
Due date: Tuesday, Nov. 5

- **Q.1.** It is required to design a circuit that computes the results of election and determines the winner. It is assumed that there are four members competing in the election with the following codes: Member 1: 00, Member 2: 01, Member 3: 10, and Member 4: 11. Assume that the number of votes to be counted will be given to the circuit when a *Start* input is set. Assume for simplicity that the maximum number of votes to be counted is 63. Assume that votes will be given to the circuit one vote at a time before the rising edge of each clock cycle. Once the circuit finishes computation, it will assert a *Done* signal and will generate a 2-bit output indicating the code of the winner. In case there is a tie, a Tie signal is set to 1.
 - (i) Develop an ASMD chart for the circuit.

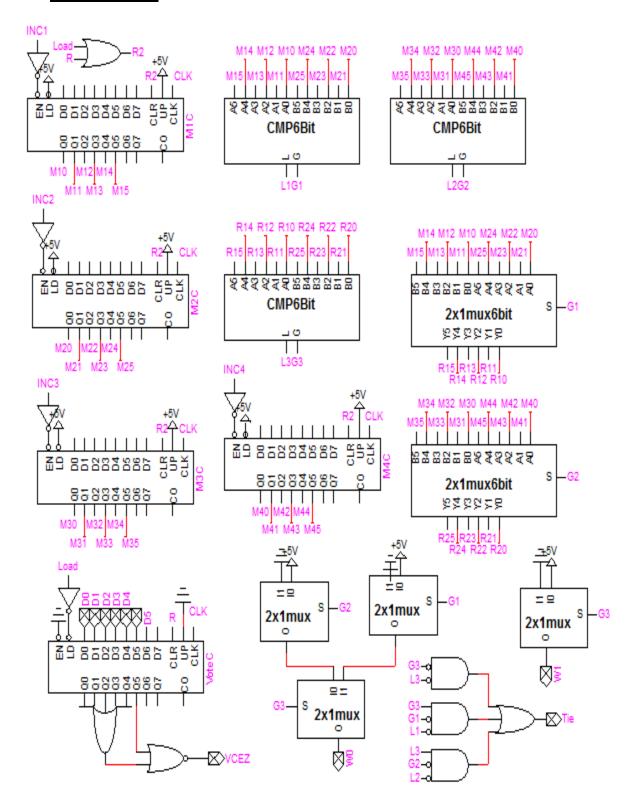


(ii) Show the design of the data-path and control unit of the circuit.

Block Diagram:



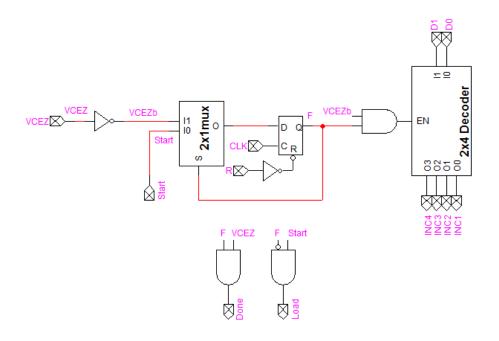
Data Path Unit:



Control Unit:

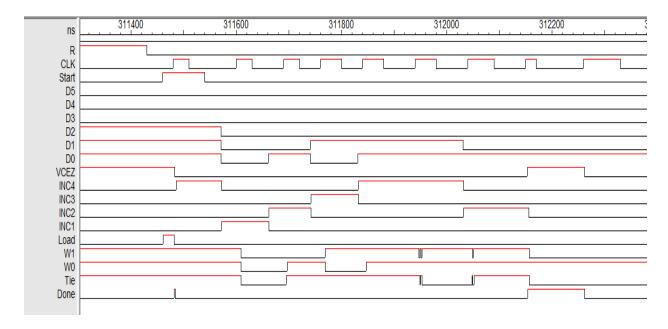
C.S.	Input				N.S.	Output					
	Start	Data[1]	Data[0]	VCEZ		Load	INC1	INC2	INC3	INC4	Done
S0	0	X	X	X	S0	0	0	0	0	0	0
S0	1	X	X	X	S1	1	0	0	0	0	0
S1	X	0	0	0	S1	0	1	0	0	0	0
S1	X	0	1	0	S1	0	0	1	0	0	0
S 1	X	1	0	0	S1	0	0	0	1	0	0
S1	X	1	1	0	S1	0	0	0	0	1	0
S 1	X	X	X	1	S0	0	0	0	0	0	1

State Assignment: S0=0, S1=1.



(iii) Implement the circuit and verify its correct functionality by simulation.

The simulation waveforms given below show clearly that the circuit works correctly: In the first simulation run, the number of votes is 7 and the votes applied are: 0, 1, 2, 3, 3, 1, 1. The winner is member 1.



In the second simulation run, the number of votes is 6 and the votes applied are: 2, 1, 2, 1, 3, 0. There is a tie between member 1 and member 2.

