COE 405, Term 152

Design & Modeling of Digital Systems

HW# 3

Due date: Tuesday, March 1

Q.1. It is required to design a circuit that receives an array of n unsigned 4-bit numbers along with a 4-bit target value and counts the number of data elements that are greater or equal to the target value. Assume that once the user presses *Start* he will also supply the number of elements in the array n ($n \leq 15$) through input1 and the target value through input2 in the same cycle. Assume that input2 will hold the target value until the circuit finishes its operation. In the next n consecutive cycles, the user will provide the n data elements through input1. Once the circuit finishes computation, it will assert a *Done* signal and will generate a 4-bit output indicating the count of the number of elements in the array $\geq$ target value. The *Done* signal and the result will remain valid unless the user resets the machine or asserts the *Start* signal.

(i) Develop an ASMD chart for the circuit.

(ii) Show a block diagram for the datapath and control unit interface.

(iii) Show the design of the data-path and control unit of the circuit.

(iv) Implement the circuit using logicworks and verify its correct functionality by simulation.