COE 405, Term 131

Design & Modeling of Digital Systems

HW# 3

Due date: Tuesday, Nov. 5

Q.1. It is required to design a circuit that computes the results of election and determines the winner. It is assumed that there are four members competing in the election with the following codes: Member 1: 00, Member 2: 01, Member 3: 10, and Member 4: 11. Assume that the number of votes to be counted will be given to the circuit when a *Start* input is set. Assume for simplicity that the maximum number of votes to be counted is 63. Assume that votes will be given to the circuit one vote at a time before the rising edge of each clock cycle. Once the circuit finishes computation, it will assert a *Done* signal and will generate a 2-bit output indicating the code of the winner. In case there is a tie, a Tie signal is set to 1.

(i) Develop an ASMD chart for the circuit.

(ii) Show the design of the data-path and control unit of the circuit.

(iii) Implement the circuit and verify its correct functionality by simulation.