# COE 405, Term 122

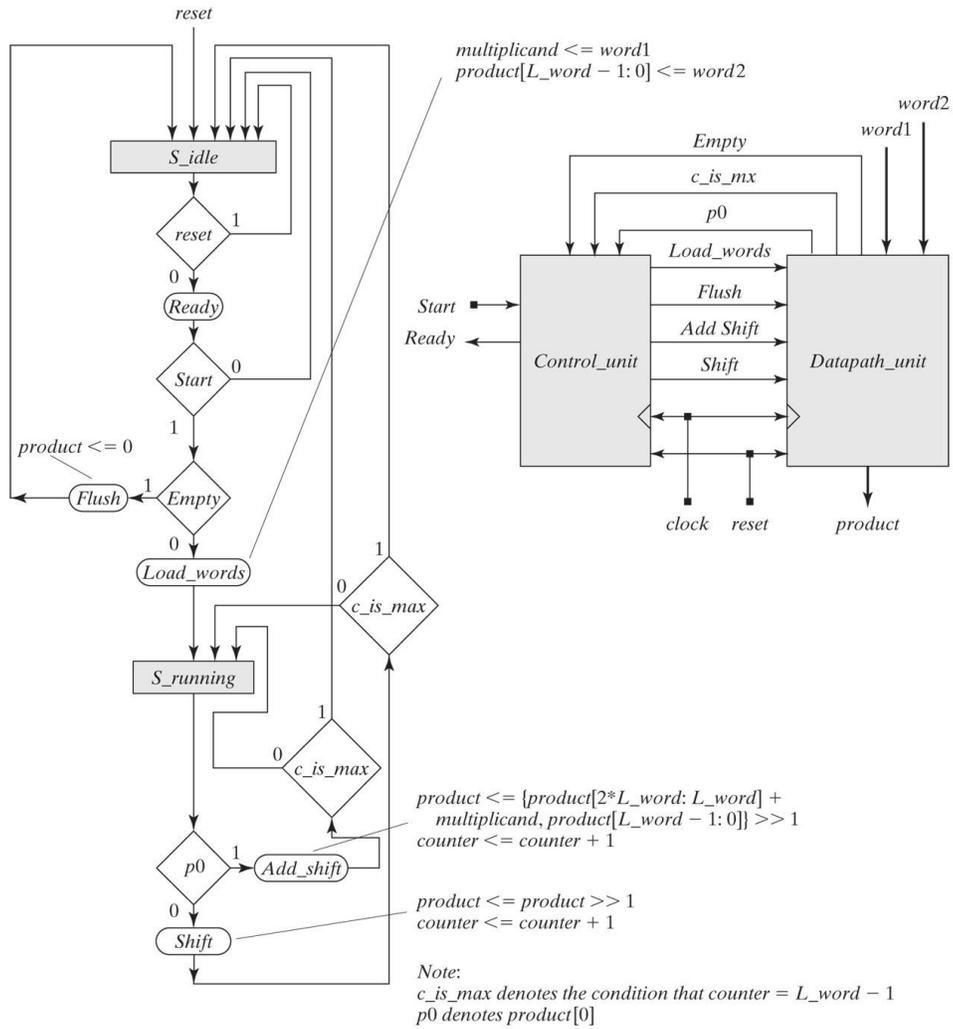## Design & Modeling of Digital Systems

HW# 3

Due date: Saturday, March 16

Q.1. The block diagram below shows the datapath and controller for a machine that transfers two 4-bit signed numbers in 2's complement representation into registers AR and BR, divides the number in AR by 2 and transfers the result to register CR if the number in AR is negative, multiplies the number in BR by 2 and transfers the result to register CR if the number in AR is positive but non-zero, and if the number in AR is zero, clears register CR to 0.
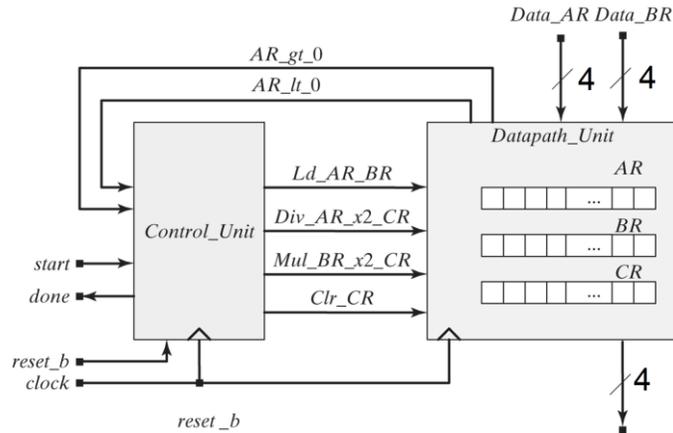
(i) Develop an ASMD chart for the machine.

(ii) Show the design of the data-path and control unit of the machine.

(iii) Implement the machine and verify its correct functionality by simulation.

Q.2. It is required to design an unsigned 4-bit sequential multiplier. The multiplier is assumed to have an 8-bit register to hold the result, a 4-bit register to hold the multiplicand and a 3-bit counter. When reset is 1, the multiplicand, the product and counter registers are reset. When operation is started, the multiplicand register is loaded with word1 while the least significant 4-bits of the product are loaded with word2. The block diagram and the ASMD chart of the sequential multiplier are given below. *Ready* signals that the unit is ready to accept a command to multiply. If word1 or word2 are 0, *Empty* is set to 1. *Flush* loads the product with 0. *C_is_mx* is set when the counter is equal to 3. *P0* is the least significant bit of the product i.e. product[0].

reset

multiplicand $<=$ word1
product$[L\_word - 1 : 0] <=$ word2

word2
word1

S_idle

Empty
c_is_mx
p0
Load_words
Flush
Add Shift
Shift

Start
Ready

Control_unit

Datapath_unit

clock   reset   product

reset   1

0
Ready

Start   0

1

product $<= 0$

Flush   1   Empty

0
Load_words

1

0   c_is_max

S_running

1

0   c_is_max

product $<= \{$product$[2*L\_word : L\_word] +$
    multiplicand, product$[L\_word - 1 : 0]\} >> 1$
counter $<=$ counter $+ 1$

p0   1   Add_shift

0

Shift

product $<=$ product $>> 1$
counter $<=$ counter $+ 1$

Note:
c_is_max denotes the condition that counter $= L\_word - 1$
p0 denotes product$[0]$

(i) Show the design of the data-path and control unit of the 4-bit sequential multiplier.

(ii) Implement the machine and verify its correct functionality by simulation.