COE 405, Term 131

Design & Modeling of Digital Systems

HW# 2 Solution

Due date: Wednesday, October 9

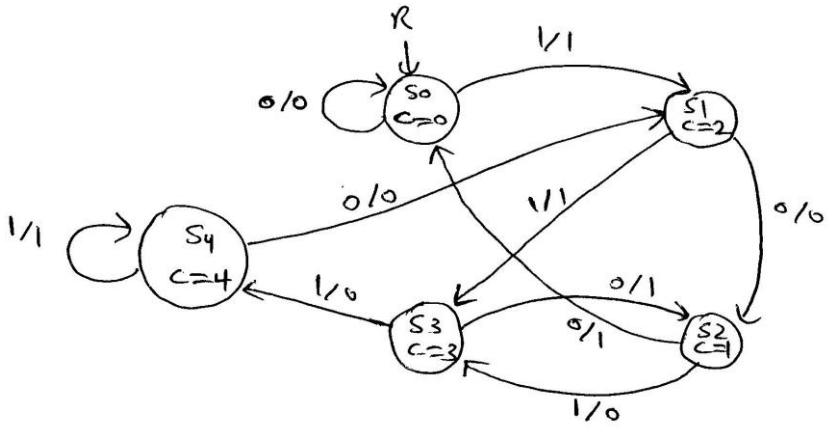
Q.1. It is required to design a sequential circuit that has a single input X and a single output Y. The circuit receives an unsigned number serially through the input X from the least significant bit (LSB) to the most significant bit (MSB), and computes the equation 5*X and generates the output serially from the least significant bit to the most significant bit. The circuit has an additional reset input R which resets the circuit into an initial state. The following are examples of input and output data:

Examples:

		LSB				MSB	
Input	X	0	1	1	0	0	Input=6
Output	Y	0	1	1	1	1	Output=30

		LSB				MSB	
Input	X	1	1	0	0	0	Input=3
Output	Y	1	1	1	1	0	Output=15

(i) Draw the state diagram of the circuit assuming a **Mealy** model.

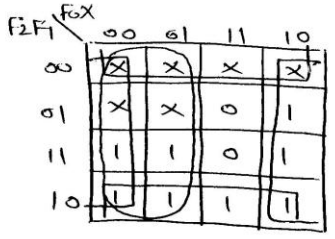


(ii) Implement the circuit using D-FFs.

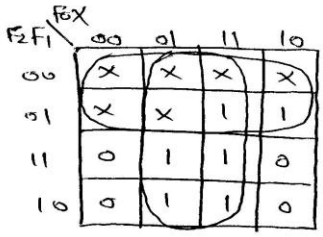
We implement the circuit using the following state assignment:

$S_0 = 100$, $S_1 = 110$, $S_2 = 101$, $S_3 = 111$, $S_4 = 011$

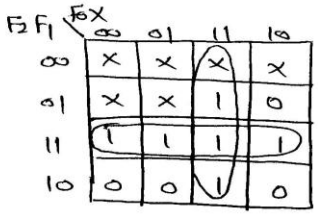
	C.S. $F_2\ F_1\ F_0$	input x	N.S $F_2^+\ F_1^+\ F_0^+$	output y
S_0	1 0 0	0	1 0 0	0
	1 0 0	1	1 1 0	1
S_1	1 1 0	0	1 0 1	0
	1 1 0	1	1 1 1	1
S_2	1 0 1	0	1 0 0	1
	1 0 1	1	1 1 1	0
S_3	1 1 1	0	1 0 1	1
	1 1 1	1	0 1 1	0
S_4	0 1 1	0	1 1 0	0
	0 1 1	1	0 1 1	1



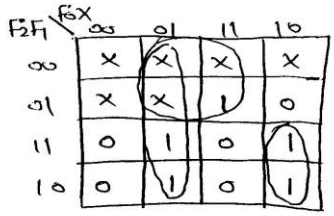
$F_2^+ = \bar{F_1} + \bar{F_0} + \bar{x}$



$F_1^+ = \bar{F_2} + x$

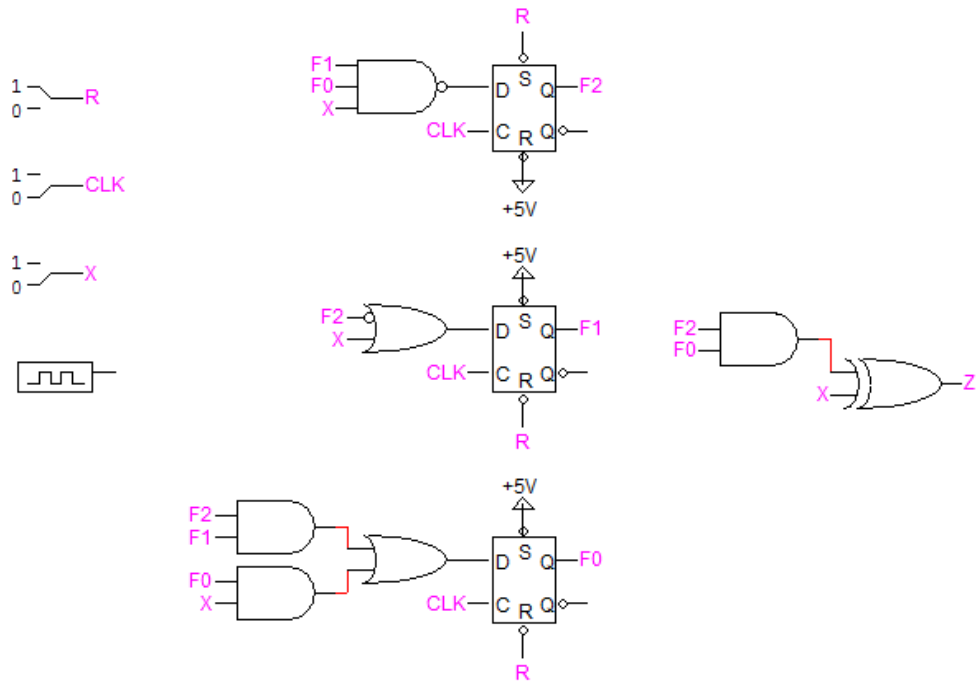


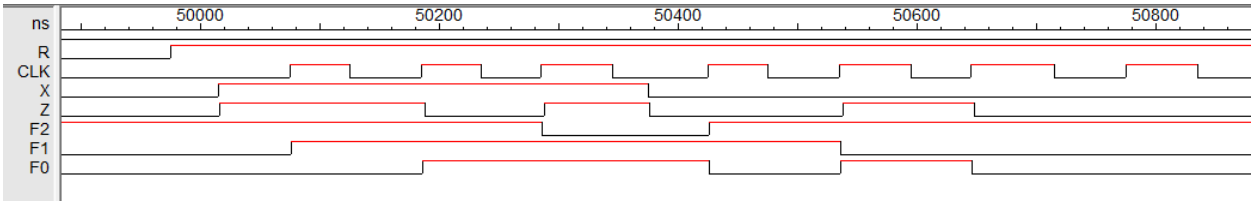
$F_0^+ = F_2F_1 + F_0x$



$$z = \bar{F_2}x + \bar{F_0}x + F_2F_0\bar{x}$$
$$= x(\bar{F_2} + \bar{F_0}) + \bar{x}(F_2F_0)$$
$$= x \oplus F_2F_0$$

(iii) Verify the correctness of your circuit by simulation.



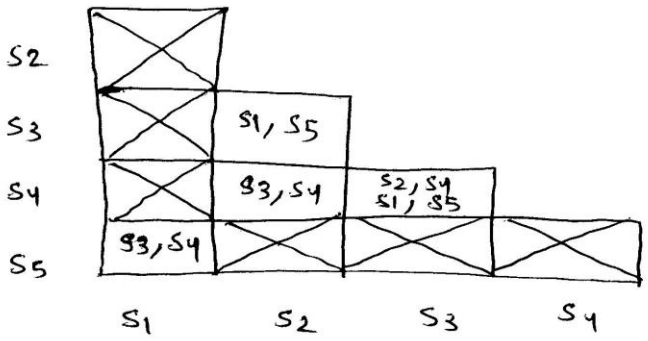


It is clear from simulations that the circuit is working properly as for the input X=111=7, the output produced is Y=110001=35.

Q.2. Consider the given FSM that has 5 states, one input (X) and one output (Z), represented by the following state table:

Present State	**Next State, Z**	
	X=0	**X=1**
S1	S3, 1	S5, 0
S2	S3, 0	S5, 1
S3	S2, 0	S1, 1
S4	S4, 0	S5, 1
S5	S4, 1	S1, 0

(i) Determine the equivalent states.



Equivalent states : (S_1, S_5), (S_2, S_3)
(S_2, S_4), (S_3, S_4)

$\Rightarrow$ (S_1, S_5) , (S_2, S_3, S_4)

(ii) Reduce the state table into the minimum number of states and show the reduced state table.

Reduced State table:

P.S.	N.S, Z	
	X = 0	X = 1
S15	S234, 1	S15, 0
S234	S234, 0	S15, 1

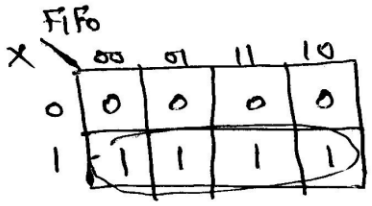
Q.3. Consider the given FSM that has 4 states, one input (X) and one output (Z), represented by the following state table:

Present State	**Next State, Z**	
	X=0	**X=1**
S0	S0, 0	S1, 0
S1	S2, 0	S3, 0
S2	S0, 0	S1, 1
S3	S2, 0	S3, 0

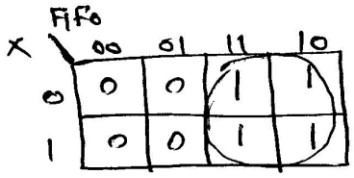
(i) Implement the FSM using the following state assignment: S0=00, S1=10, S2=01, S3=11.

$S_0 = 00,\ S_1 = 10,\ S_2 = 01,\ S_3 = 11$

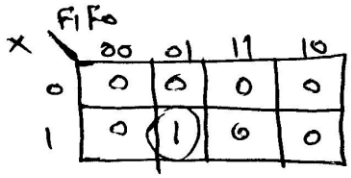
P.S. F_1F_0	N.S., Z $X=0$	$X=1$
00	00, 0	10, 0
10	01, 0	11, 0
01	00, 0	10, 1
11	01, 0	11, 0



$F_1^+ = X$



$F_0^+ = F_1$



$Z = X \bar{F}_1 F_0$

(ii) Implement the FSM using the following state assignment: S0=11, S1=01, S2=00, S3=10.

$S_0 = 11$, $S_1 = 01$, $S_2 = 00$, $S_3 = 10$

P.S. $F_1 F_0$	N.S., Z $x=0$	$x=1$
1 1	11 , 0	01, 0
0 1	00 , 0	10 , 0
0 0	11 , 0	01 , 1
1 0	00 , 0	10 , 0

x \ F_1F_0	00	01	11	10
0	1	0	1	0
1	0	1	0	1

$$F_1^+ = \overline{x \oplus F_1 \oplus F_0}$$
$$= x \oplus \overline{F_1 \oplus F_0}$$

x \ F_1F_0	00	01	11	10
0	1	0	1	0
1	1	0	1	0

$$F_0^+ = \overline{F_1 \oplus F_0}$$

x \ F_1F_0	00	01	11	10
0	0	0	0	0
1	1	0	0	0

$$Z = x \bar{F_1} \bar{F_0}$$

(iii) Verify that the two circuits are equivalent by simulation by applying the following input sequence: {0,1,0,1,1,0,1,0,1,0,0}.