COE 405, Term 122

Design & Modeling of Digital Systems

HW# 2 Solution

Due date: Monday, March 4

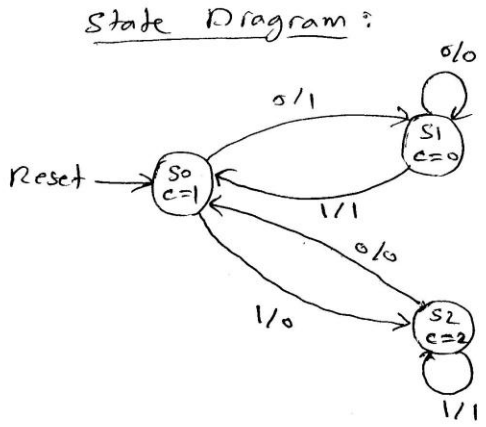
Q.1. It is required to design a sequential circuit that has a single input X and a single output Y. The circuit receives an unsigned number serially through the input X from the least significant bit (LSB) to the most significant bit (MSB), and computes the equation 3*X+1 and generates the output serially from the least significant bit to the most significant bit. The circuit has an additional reset input R which resets the circuit into an initial state. The following are examples of input and output data:

Examples:

		LSB				MSB	
Input	X	0	1	1	0	0	Input=6
Output	Y	1	1	0	0	1	Output=19

		LSB				MSB	
Input	X	1	1	0	0	0	Input=3
Output	Y	0	1	0	1	0	Output=10

(i) Draw the state diagram of the circuit assuming a **Mealy** model.

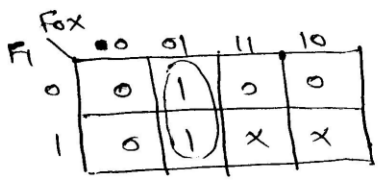


(ii) Implement the circuit using D-FFs.

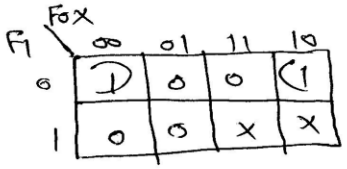
Circuit Implementation:

Since we have 3 states, we need 2 flip-flops. Let us use the following state assignment: $S_0 = 00$, $S_1 = 01$, $S_2 = 10$.

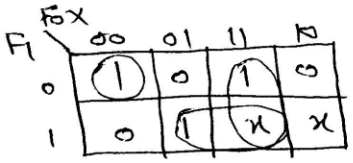
F_1	F_0	x	F_1^+	F_0^+	Z
0	0	0	0	1	1
0	0	1	1	0	0
0	1	0	0	1	0
0	1	1	0	0	1
1	0	0	0	0	0
1	0	1	1	0	1
1	1	0	x	x	x
1	1	1	x	x	x



$D_1 = \bar{F}_0 x$



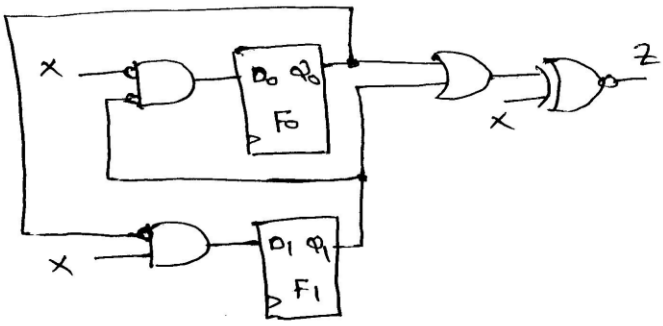
$D_0 = \bar{F}_1 \bar{x}$



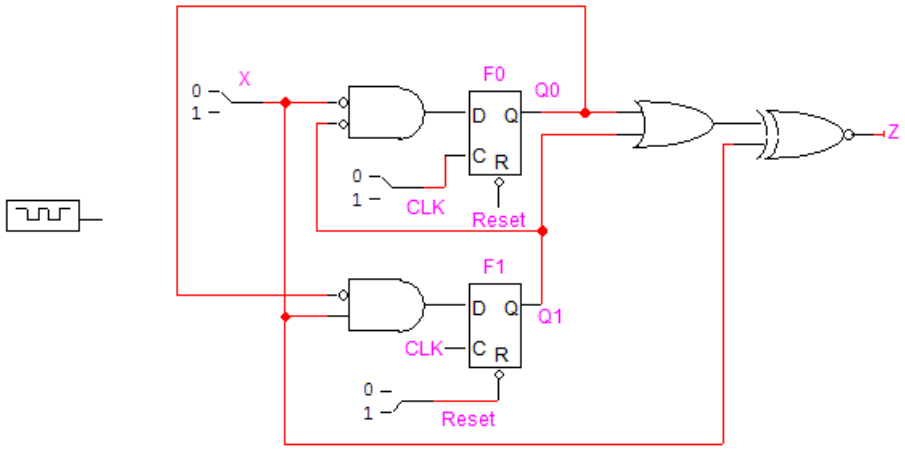
$$Z = \bar{F}_1 \bar{F}_0 \bar{x} + F_0 x + F_1 x$$

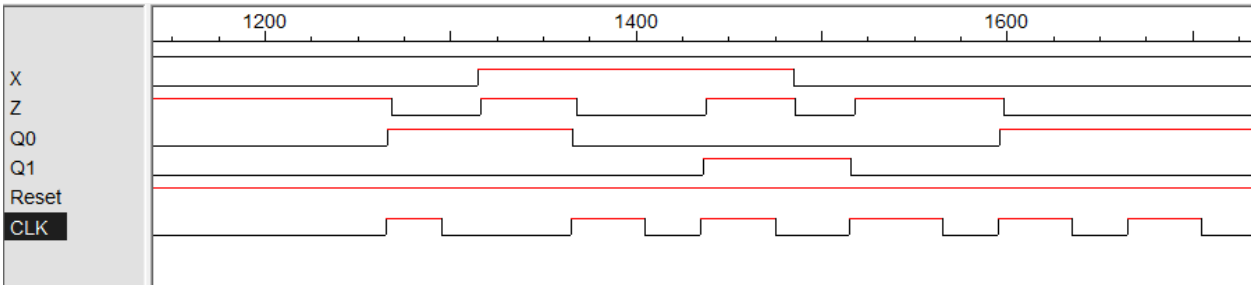
$$= \bar{F}_1 \bar{F}_0 \bar{x} + x (F_0 + F_1)$$

$$= \overline{(F_0 + F_1)}\, \bar{x} + x (F_0 + F_1)$$



(iii) Verify the correctness of your circuit by simulation.

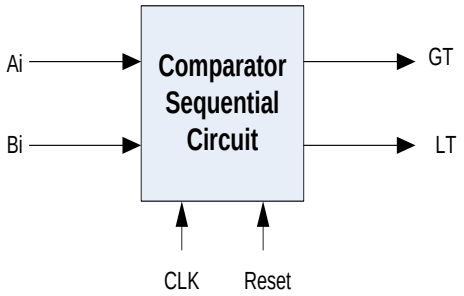




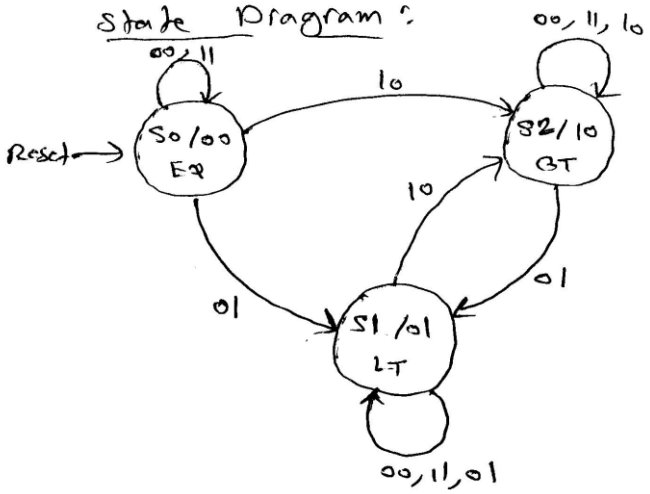
It can be seen that the circuit is working correctly. The input X=0110=6 is applied and the output Z=10011=19 is produced.

Q.2. It is required to design a sequential circuit that compares two n-bit numbers $A=A_{n-1}A_2A_1A_0$ and $B=B_{n-1}B_2B_1B_0$, applied to the sequential circuit serially from the least significant bits to the most significant bits. The circuit produces two outputs GT and LT. If A>B, then the output signal GT is set to 1 and LT is set to 0. If A<B, then the output signal LT is set to 1, and GT is set to 0. Otherwise, both signals will be set to 0, which indicates that the two numbers are equal (i.e. A=B). Assume the existence of a reset input to reset the machine to a reset state. The following is an example of the input and output streams:

		LSB MSB
Input	**A**	0 1 0 0 1 0 1 0
	B	0 0 0 1 1 0 1 0
Output	**GT**	0 0 1 1 0 0 0 0
	LT	0 0 0 0 1 1 1 1



(i) Draw the state diagram of the circuit assuming a **Moore** model.

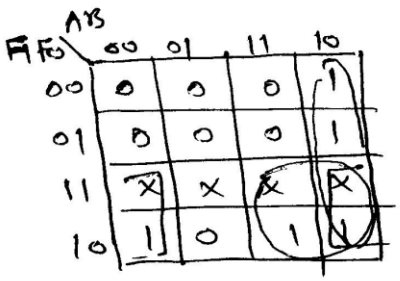


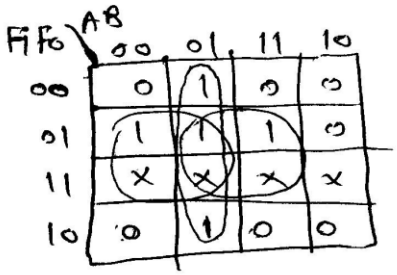
(ii) Implement the circuit using D-FFs.

Circuit Implementation:

Since we have 3 states, we need two flip flops, F_1 and F_0.
We use the state assignment to be the same as the output for each state
i.e. $S_0 = 00$, $S_1 = 01$, $S_2 = 10$

F_1	F_0	A	B	F_1^+	F_0^+	GT	LT
0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0
0	0	1	0	1	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	0	1
0	1	1	0	1	0	0	1
0	1	1	1	0	1	0	1
1	0	0	0	1	0	1	0
1	0	0	1	0	1	1	0
1	0	1	0	1	0	1	0
1	0	1	1	1	0	1	0
1	1	0	0	x	x	x	x
1	1	0	1	x	x	x	x
1	1	1	0	x	x	x	x
1	1	1	1	x	x	x	x



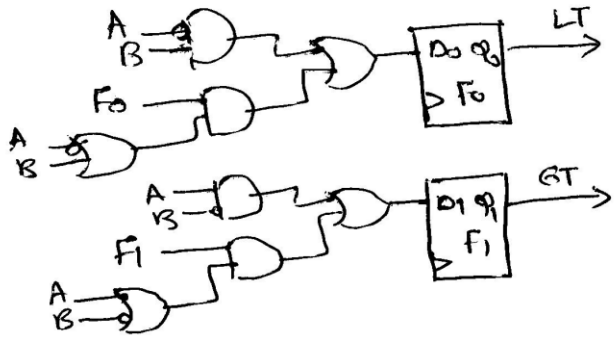


$$F_1^+ = A\bar{B} + F_1\bar{B} + F_1 A$$

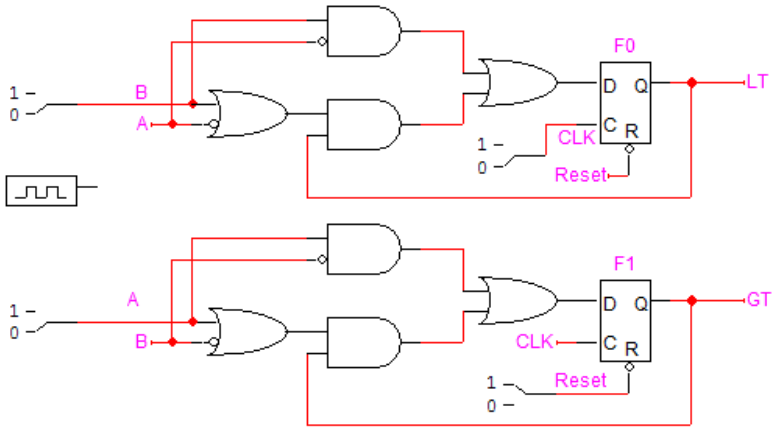
$$= A\bar{B} + F_1(A + \bar{B})$$

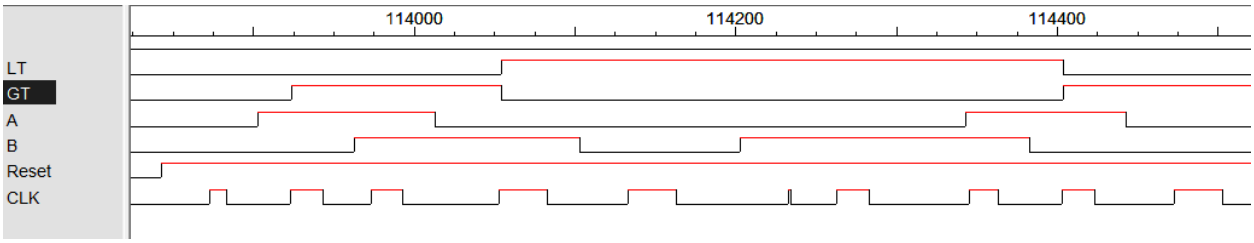
$$F_0^+ = \bar{A}B + F_0\bar{A} + F_0 B$$

$$= \bar{A}B + F_0(\bar{A} + B)$$



(iii) Verify the correctness of your circuit by simulation.

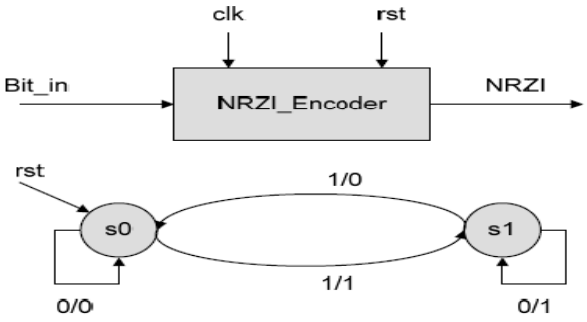




Simulation results verify the correct operation of the circuit.

Q.3. It is required to design a sequential circuit that implements a NRZI line encoder.

(i) Draw the state diagram of the circuit assuming a **Mealy** model.



(ii) Implement the circuit using D-FFs.

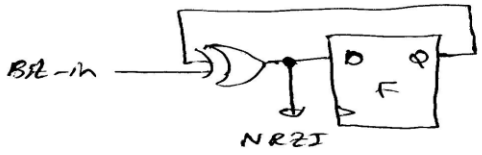
Circuit Implementation :

Since we have two states, we need one flip flop, F.
We use the state assignment $S0 = 0$, $S1 = 1$

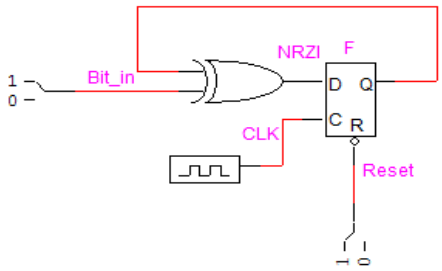
F	Bit_in	F^+	NRZI
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

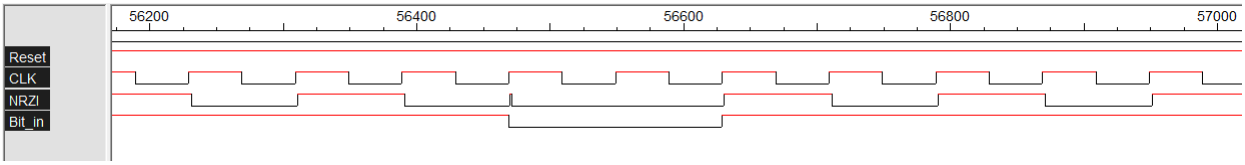
F \ Bit_in	0	1
0	0	1
1	1	0

$D = F \oplus Bit\_in$ $\quad NRZI = F \oplus Bit\_in$



(iii) Verify the correctness of your circuit by simulation.





Simulation results verify the correct operation of the circuit.

Q.4. Consider the given FSM that has 5 states, one input (X) and one output (Z), represented by the following state table:

Present State	**Next State, Z**	
	X=0	**X=1**
S0	S2, 1	S4, 0
S1	S2, 0	S4, 1
S2	S1, 0	S0, 1
S3	S3, 0	S4, 1
S4	S3, 1	S0, 0

(i) Determine the equivalent states.

Implication Chart:

S1	x			
S2	x	(S0,S4)		
S3	x	(S2, S3)	(S1,S3), (S0,S4)	
S4	(S2, S3)	x	x	x
	S0	S1	S2	S3

Thus, equivalent states are: (S1, S2, S3), (S0, S4)

(ii) Reduce the state table into the minimum number of states and show the reduced state table.

Reduced State Table:

Present State	**Next State, Z**	
	X=0	**X=1**
$S_{0,4}$	$S_{1,2,3}$, 1	$S_{0,4}$, 0
$S_{1,2,3}$	$S_{1,2,3}$, 0	$S_{0,4}$, 1