COE 405, Term 131

Design & Modeling of Digital Systems

HW# 2

Due date: Wednesday, October 9

Q.1. It is required to design a sequential circuit that has a single input X and a single output Y. The circuit receives an unsigned number serially through the input X from the least significant bit (LSB) to the most significant bit (MSB), and computes the equation 5*X and generates the output serially from the least significant bit to the most significant bit. The circuit has an additional reset input R which resets the circuit into an initial state. The following are examples of input and output data:

Examples:

		LSB				MSB	
Input	X	0	1	1	0	0	Input=6
Output	Y	0	1	1	1	1	Output=30

		LSB				MSB	
Input	X	1	1	0	0	0	Input=3
Output	Y	1	1	1	1	0	Output=15

(i) Draw the state diagram of the circuit assuming a **Mealy** model.

(ii) Implement the circuit using D-FFs.

(iii) Verify the correctness of your circuit by simulation.

Q.2. Consider the given FSM that has 5 states, one input (X) and one output (Z), represented by the following state table:

Present State	**Next State, Z**	
	X=0	**X=1**
S1	S3, 1	S5, 0
S2	S3, 0	S5, 1
S3	S2, 0	S1, 1
S4	S4, 0	S5, 1
S5	S4, 1	S1, 0

(i) Determine the equivalent states.

(ii) Reduce the state table into the minimum number of states and show the reduced state table.

Q.3. Consider the given FSM that has 4 states, one input (X) and one output (Z), represented by the following state table:

Present State	**Next State, Z**	
	X=0	**X=1**
S0	S0, 0	S1, 0
S1	S2, 0	S3, 0
S2	S0, 0	S1, 1
S3	S2, 0	S3, 0

(i) Implement the FSM using the following state assignment: S0=00, S1=10, S2=01, S3=11.

(ii) Implement the FSM using the following state assignment: S0=11, S1=01, S2=00, S3=10.

(iii) Verify that the two circuits are equivalent by simulation by applying the following input sequence: {0,1,0,1,1,0,1,0,1,0,0}.