COE 405, Term 122

Design & Modeling of Digital Systems

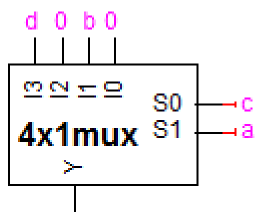
HW# 1 Solution

Due date: Monday, Feb. 18

Q.1. Consider the two functions f=(a+bc)(a'+cd) and g=(a+b)(c+d).

(i) Implement the function f using a single 4x1 MUX.

F = a' c' [0] + a' c [b] + a c' [0] + a c [d]



(ii) Compute the complement of f.

F' = a' c' [1] + a' c [b'] + a c' [1] + a c [d']

(iii) Compute the function f⊕g based on orthonormal basis expansion.

F = a' c' [0] + a' c [b] + a c' [0] + a c [d]

G = a' c' [b d] + a' c [b] + a c' [d] + a c [1]

F⊕G= a' c' [b d] + a' c [0] + a c' [d] + a c [d']

Q.2. You are required to design a circuit that computes the remainder of dividing a 4-bit number by 3. For example, if the input is 1010 the circuit produces a remainder output of 01 and if the input is 1111 the circuit produces an output of 00.

(i) Derive the truth table of your circuit.

A_1	A_0	B_1	B_0	R_1	R_0
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	0	0
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	1	0	1
1	0	0	0	1	0
1	0	0	1	0	0
1	0	1	0	0	1
1	0	1	1	1	0
1	1	0	0	0	0
1	1	0	1	0	1
1	1	1	0	1	0
1	1	1	1	0	0

(ii) Using k-map simplification, find the minimum sum-of-products expressions for each of the output signals.

a.

A1 A0 \ B1 B0	00	01	11	10
00	0	1	0	0
01	1	0	1	0
11	0	1	0	0
10	0	0	0	1

R_0

A1 A0 \ B1 B0	00	01	11	10
00	0	0	0	1
01	0	1	0	0
11	0	0	0	1
10	1	0	1	0

R_1

$R_0 = A_1' A_0' B_1' B_0 + A_1' A_0 B_1 B_0 + A_1' A_0 B_1' B_0' + A_1 A_0 B_1' B_0 + A_1 A_0' B_1 B_0'$

$R_1 = A_1 A_0 B_1 B_0' + A_1' A_0' B_1 B_0' + A_1 A_0' B_1' B_0' + A_1 A_0' B_1 B_0 + A_1' A_0 B_1' B_0$

(iii) Perform multilevel optimizations if possible.

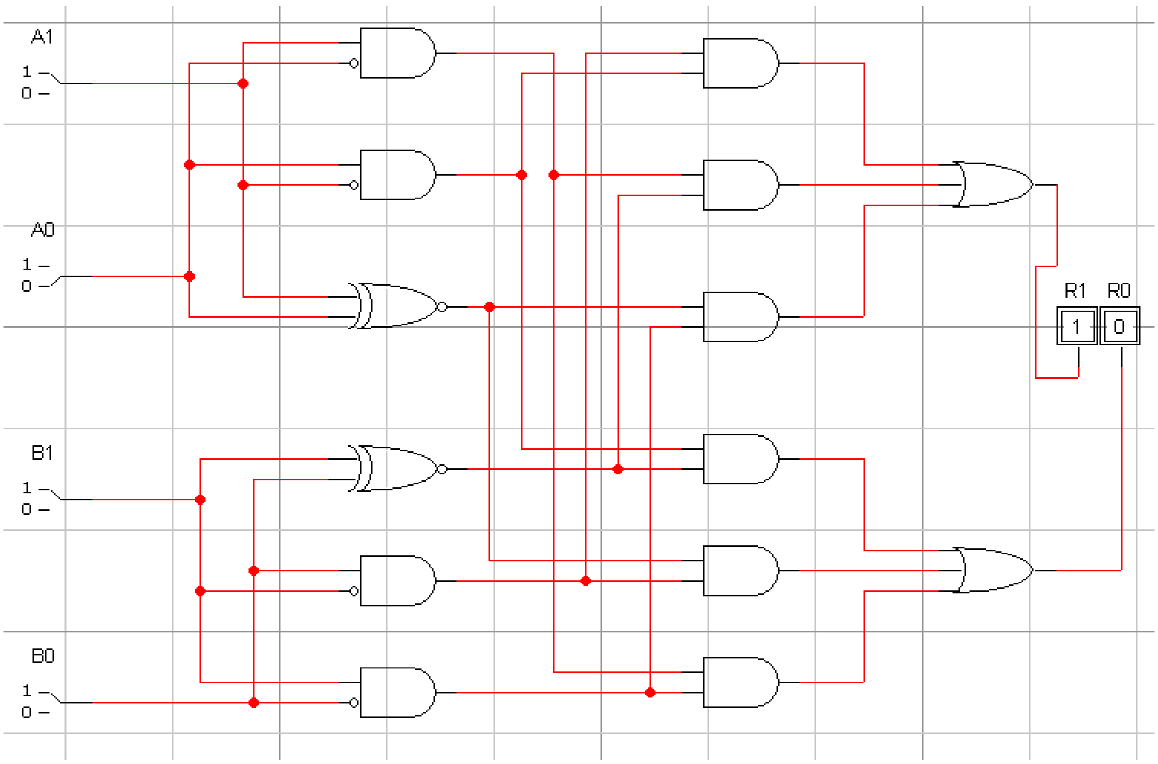
$$R_0 = A_1' A_0' B_1' B_0 + A_1' A_0 B_1 B_0 + A_1' A_0 B_1' B_0' + A_1 A_0 B_1' B_0 + A_1 A_0' B_1 B_0'$$

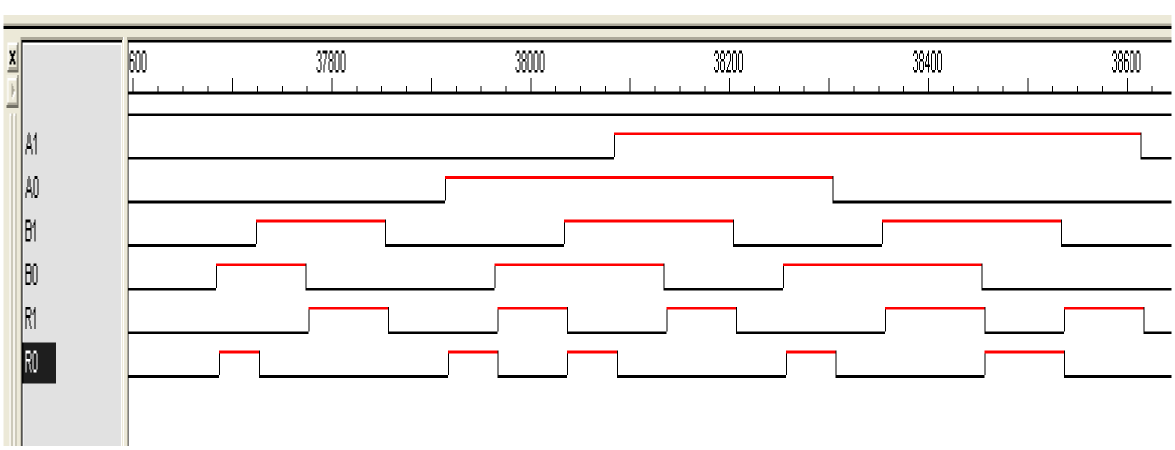
$$R_0 = A_1' A_0 (B_1 \odot B_0) + B_1' B_0 (A_1 \odot A_0) + A_1 A_0' B_1 B_0'$$

$$R_1 = A_1 A_0 B_1 B_0' + A_1' A_0' B_1 B_0' + A_1 A_0' B_1' B_0' + A_1 A_0' B_1 B_0 + A_1' A_0 B_1' B_0$$

$$R_1 = A_1 A_0' (B_1 \odot B_0) + B_1 B_0' (A_1 \odot A_0) + A_1' A_0 B_1' B_0$$

(iv) Model your circuit using logic works and verify that it is working properly by simulation. Provide a snapshot of your simulation waveform.





Q.3. You are required to design a circuit that computes the remainder of dividing a N-bit number by 3, where N is a multiple of 4-bit numbers. The design needs to be modular in such a way that you design a cell that computes the remainder of dividing a 4-bit number by 3, and use this cell to construct the required circuit.

(i) Derive the truth table of your basic cell.

The circuit will be designed such that the remainder from the previous block is passed to the next block. This works as follows:

Suppose that you have an 8-bit number A_7-A_0. Then the value of this number is $A_7 \times 2^7 + A_6 \times 2^6 + A_5 \times 2^5 + A_4 \times 2^4 + A_3 \times 2^3 + A_2 \times 2^2 + A_1 \times 2^1 + A_0 \times 2^0$.

The value of this number can be rewritten as $(A_7 \times 2^3 + A_6 \times 2^2 + A_5 \times 2^1 + A_4 \times 2^0)\, 2^4 + (A_3 \times 2^3 + A_2 \times 2^2 + A_1 \times 2^1 + A_0 \times 2^0)$.

Dividing the number $(A_3 \times 2^3 + A_2 \times 2^2 + A_1 \times 2^1 + A_0 \times 2^0)$ by 3 gives an answer = $[3xQ1 + R1]/3$.

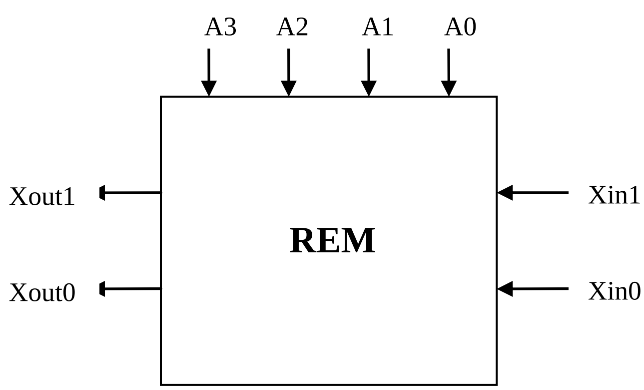
Dividing the number $(A_7 \times 2^3 + A_6 \times 2^2 + A_5 \times 2^1 + A_4 \times 2^0)$ by 3 gives an answer = $[3xQ2 + R2]/3$.

Dividing the number $(A_7 \times 2^3 + A_6 \times 2^2 + A_5 \times 2^1 + A_4 \times 2^0)\, 2^4$ by 3 gives an answer = $[3x\ Q2 \times 2^4 + (2^4 \times R2)]/3 = [3x\ Q2 \times 2^4 + 15xR2 + R2]/3$. Thus, this number will have a remainder of R2.

One can easily see now that the remainder of dividing the 8-bit number by 3 is the remainder of dividing R1+R2 by 3.

Thus, by feeding the remainder of the previous stage to the next stage, one can compute the whole number remainder.

So, the circuit will be designed as follows:



The truth table of the design is shown below:

A_3	A_2	A_1	A_0	R_1	R_0	X_{in1}	X_{in0}	X_{out1}	X_{out0}
0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	1	0	1
0	0	1	0	1	0	1	0	1	0
0	0	1	1	0	0	X	X	X	X
0	1	0	0	0	1	0	0	0	1
0	1	0	1	1	0	0	1	1	0
0	1	1	0	0	0	1	0	0	0
0	1	1	1	0	1	X	X	X	X
1	0	0	0	1	0	0	0	1	0
1	0	0	1	0	0	0	1	0	0
1	0	1	0	0	1	1	0	0	1
1	0	1	1	1	0	X	X	X	X
1	1	0	0	0	0	X	X	X	X
1	1	0	1	0	1	X	X	X	X
1	1	1	0	1	0	X	X	X	X
1	1	1	1	0	0	X	X	X	X

Note that since the reminder of the circuit depends on the current remainder and the remainder from the previous number, we need only to design another circuit that produces Xout1 and Xout0 based on R1, R0, Xin1, and Xin0 as shown below.

(ii) Using k-map simplification, find the minimum sum-of-products expressions for each of the output signals.

R1 R0 \ Xin1 Xin0	00	01	11	10
00	0	0	X	1
01	0	1	X	0
11	X	X	X	X
10	1	0	X	0

$\mathbf{X_{out1}}$

R1 R0 \ Xin1 Xin0	00	01	11	10
00	0	1	X	0
01	1	0	X	0
11	X	X	X	X
10	0	0	X	1

$\mathbf{X_{out0}}$

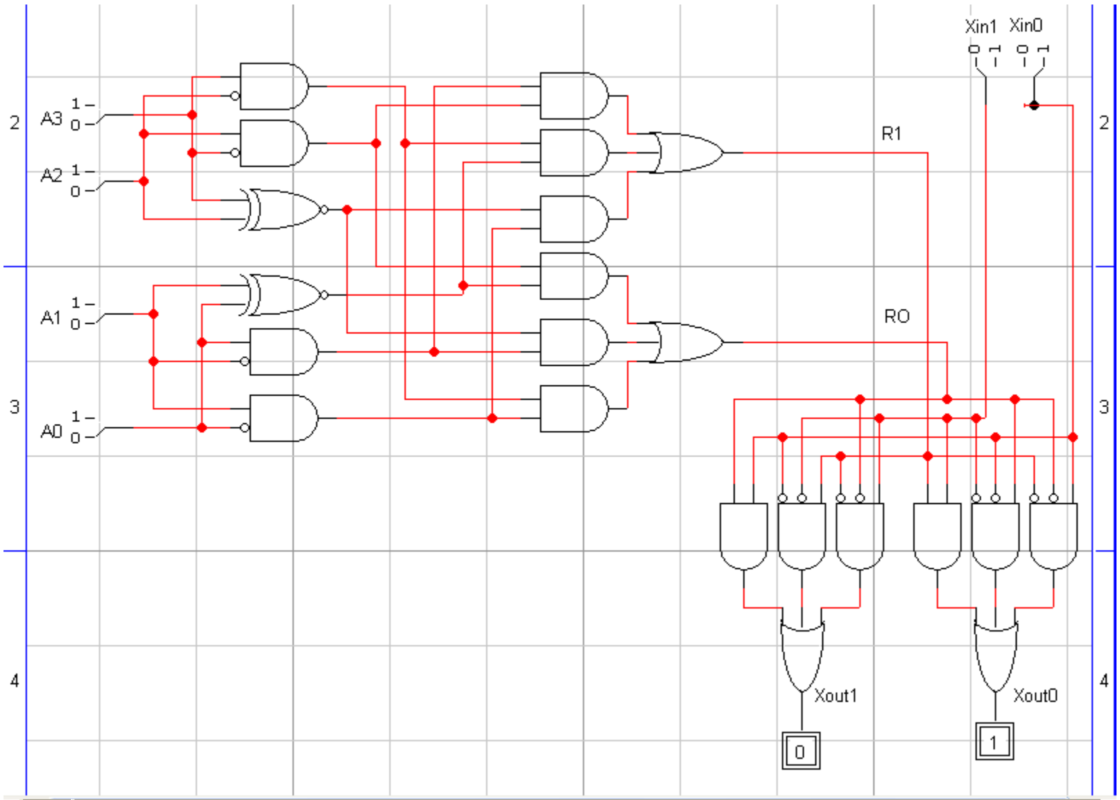
$X_{out0} = R_1\ X_{in1} + R_0\ X_{in1}'\ X_{in0}' + R_1'\ R_0'\ X_{in0}$

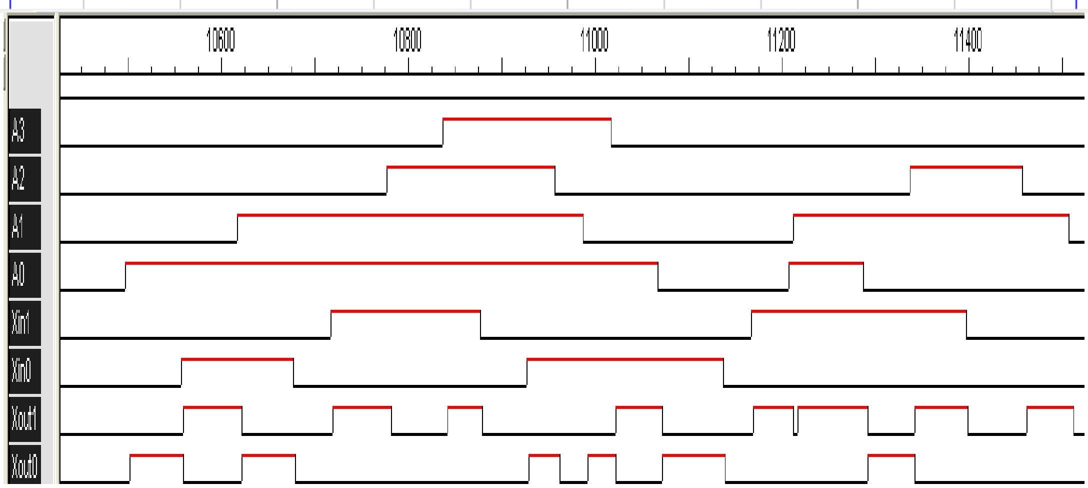
$X_{out1} = R_0\ X_{in0} + R_1\ X_{in1}'\ X_{in0}' + R_1'\ R_0'\ X_{in1}$

(iii) Perform multilevel optimizations if possible.

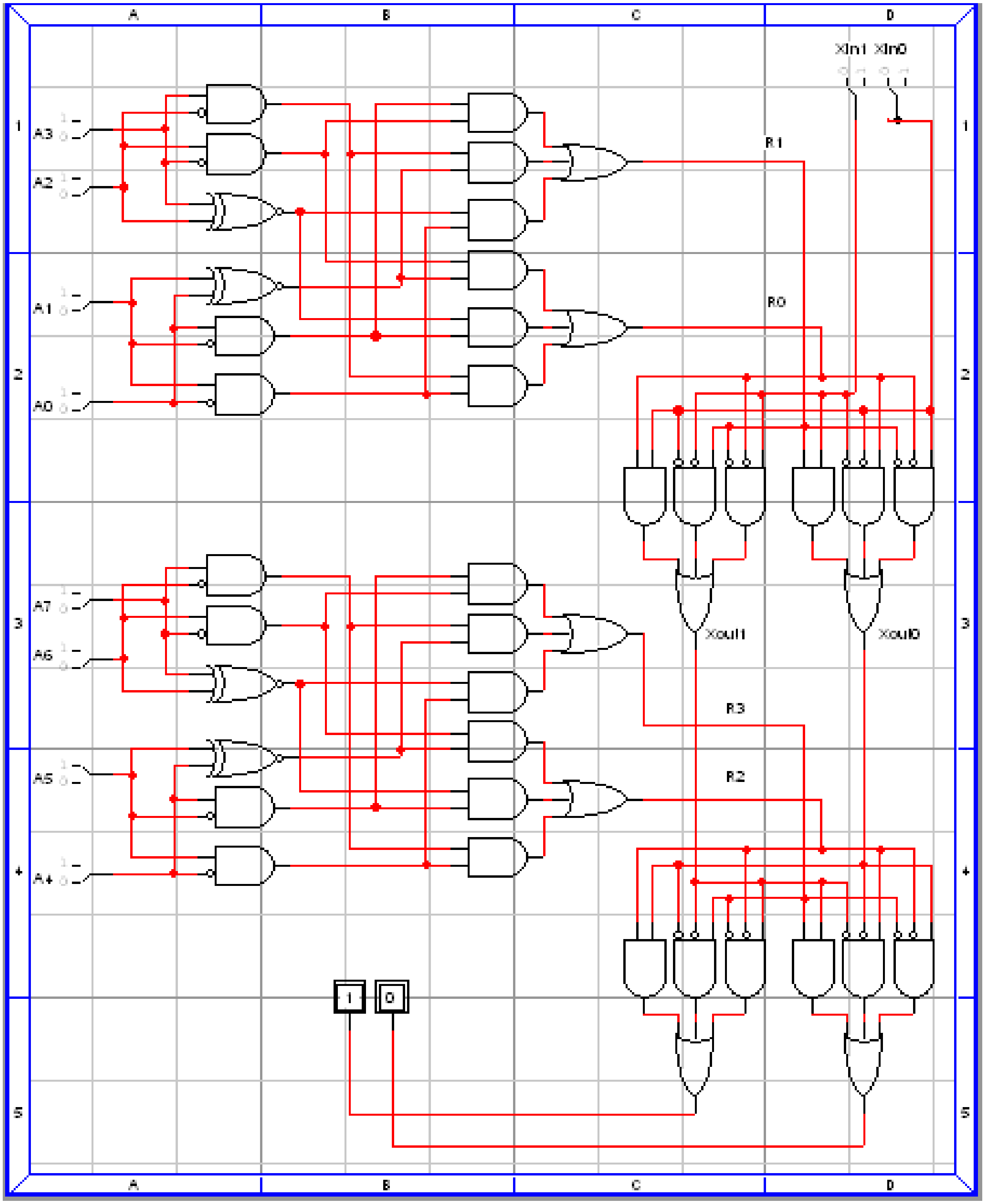
Optimizations are possible by sharing the AND gate for computing X_{in1}' X_{in0}' and the AND gate for computing R_1' R_0'.

(iv) Model your cell using logic works and verify that it is working properly by simulation. Provide a snapshot of your simulation waveform.

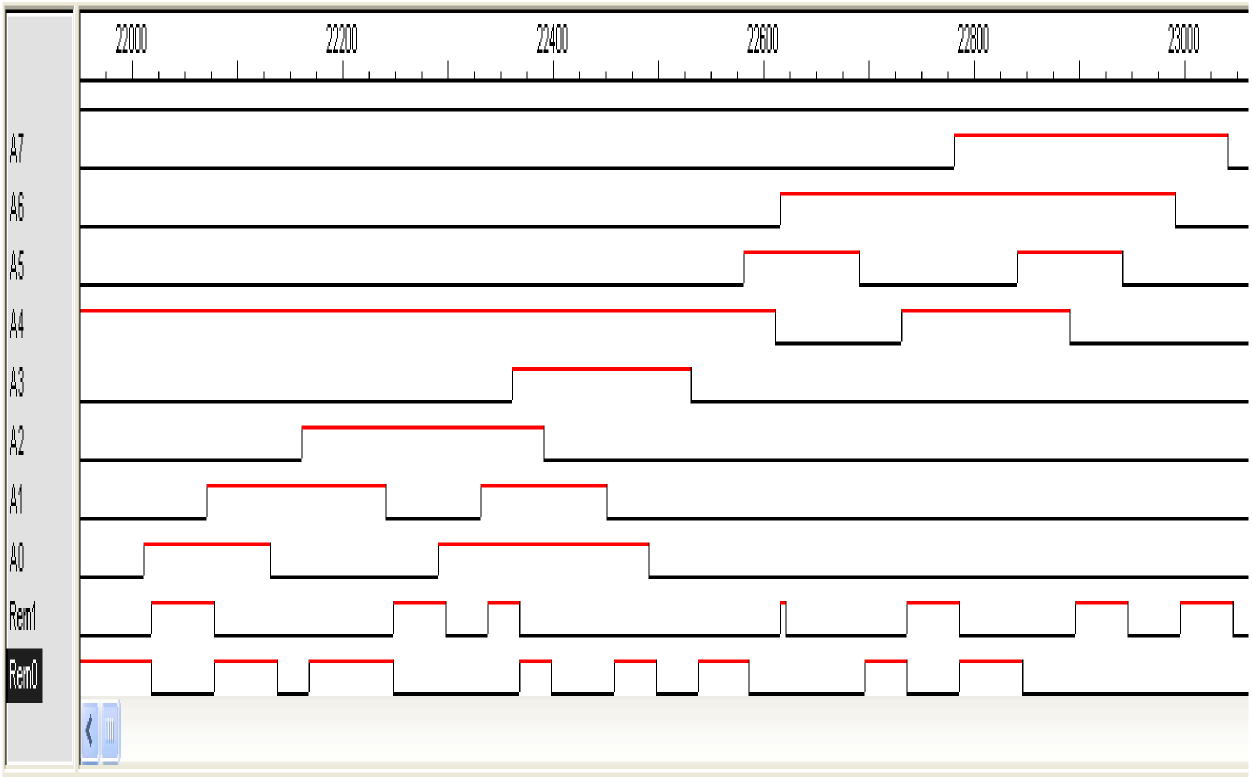




(v) Using your design cell, construct a circuit that computes the remainder of dividing an 8-bit number by 3. Verify the correct functionality of your circuit by simulation.



A
B
C
D
1
2
3
4
5
XIn1
XIn0
A3
A2
A1
A0
A7
A6
A5
A4
R1
R0
R3
R2
Xout1
Xout0
1
0


22000
22200
22400
22600
22800
23000
A7
A6
A5
A4
A3
A2
A1
A0
Rem1
Rem0