COE 405
Design & Modeling of Digital Systems

Course Project
Simple CPU Design & Modeling
Due on: Wednesday May 30, 2007

In this project, you are required to design and model a simple Central Processing Unit (CPU) interfaced with memory. You need to design the CPU to have 16 instructions. Assume that that the CPU is an 8-bit machine and has 4 general purpose registers. Make sure to select essential instructions in your design that enables you to write any needed functionality. You are free to select the needed instruction formats and whether to use fixed or variable instruction format. Assume that the address and data buss are both 8-bits. Assume that the CPU-Memory interface contains the following control signals: Read, Write, and MFC (Memory Function Complete). Both the CPU and Memory are synchronized by the same clock. When a Read or Write request is initiated by the CPU, it remains 1 until the memory indicates that it finished the requested operation by setting the MFC signal to 1. Assume that the MFC signal will remain 1 for one clock cycle. Also, assume that the MFC signal changes based on the falling edge of the clock while the CPU signals change on the rising edge of the clock.
Use **std_logic** and **std_logic_vector** for all signals in the design. Include all functions, procedures, and user-defined types and constants in a package to be used by the CPU. Make all modeled entities in the design parametrizable.

(i) Design the instruction set of your CPU showing all details about the designed instructions including instructions formats.

(ii) Write a behavioral model for the CPU modeling all its specified instruction set.

(iii) Write a behavioral model for the memory interfaced with the CPU.

(iv) Write a test bench to test your behavioral model of the CPU. The test bench should contain Memory, and an instance of the CPU under test. The assembly/machine program to be tested should be read from a file and stored in the modeled memory.

(v) Partition your CPU into a data path unit and a control unit. Write a register transfer model for the designed CPU. The data path should be described structurally while the components in the data path, i.e. ALU, registers can be described using any modeling style. The control unit is to be modeled as a finite state machine, which can be modeled in a behavioral or dataflow style.

(vi) For each entity that you model, test it independently and include simulation output indicating that it is working properly. The data-path and control unit should be tested and verified separately before they are connected together.

(vii) Test the register transfer level (RTL) model of the CPU using the same test bench used for the behavioral model. Include simulation results demonstrating correct operation of your modeled CPU.

(viii) All your models of components, datapath and control unit should be synthesizable. Synthesize each modeled component including datapath and control unit and report area and timing figures. Finally, report the area and timing figures for the whole synthesizable CPU.

(ix) *If you manage to map your CPU to an FPGA and demonstrate its proper operation, you will get a* ***5% bonus*** *from your total mark in the course.*

This project can be conducted by a team of a maximum of three students. Each team should assign a project leader who manages the project and partitions the project tasks among the team members. All team members are responsible about all tasks of the project and should collaborate to achieve a successful project. You are required to understand all the work done in the project, the part you do and the part done by the other team members.

Clearly state your assumptions and have your design well documented. Write a professional report indicating all design stages, modeling and testing of each component and the final design. Include both a hard copy and a soft copy of your report and all VHDL files. All team members are required to make a demo of their project in the project due date. The grading policy for the project is shown below:

Grading Criteria	**Mark**
CPU Instruction Set Design	10
Memory interface Modeling and Test	5
CPU Test Bench	5
CPU Behavioral Description & Test	25
Data-path Design, Modeling, Synthesis & Test	20
Control Unit Design, Modeling, Synthesis & Test	20
RTL CPU Modeling, Synthesis & Test	10
Report Organization	5
Total	100