Nov. 9, 2013

COMPUTER ENGINEERING DEPARTMENT

COE 405

DESIGN & MODELING OF DIGITAL SYSTEMS

Midterm Exam

First Semester (131)

Time: 1:30-4:00 PM

OPEN BOOK EXAM

Student Name : __KEY_____

Student ID. : _____

Question	Max Points	Score
Q1	20	
Q2	15	
Q3	10	
Q4	40	
Q5	15	
Total	100	

Dr. Aiman El-Maleh

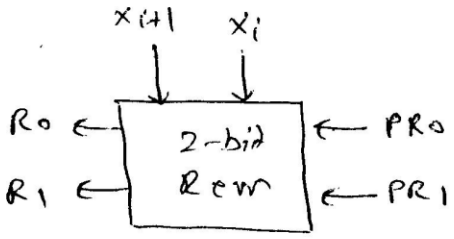
[20 Points]

(Q1) It is required to design an **iterative** combinational circuit that receives an **n-bit** number X and computes the remainder of dividing this number by 3. A 4-bit number X can be written as X=X2*4+X1, where X1 is X[1:0] and X2 is X[3:2]. The remainder of dividing X by 3 can be computed by finding the remainder of dividing (R1+R2) by 3, where R1 is the remainder of dividing X2*4 by 3 and R2 is the the remainder of dividing X1 by 3. It should be observed that the remainder of dividing X2*4 by 3 is equal to the remainder of dividing X2 by 3.

(i) Design an iterative cell that receives a 2-bit input number and the remainder of the previous 2 bits and computes the remainder of the 4-bits. Show the truth table of your circuit. You do not need to implement the circuit.

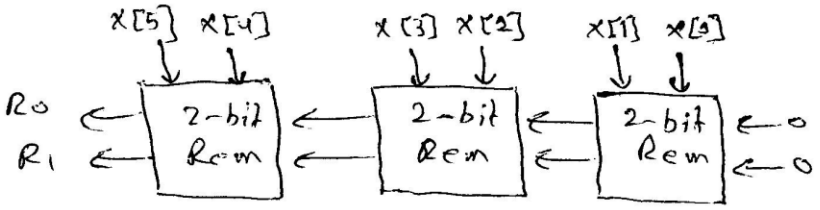
(ii) Show the block diagram for computing the remainder of dividing a 6-bit number by 3.

(i)



PR_1	PR_0	X_{i+1}	X_i	R_1	R_0
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	0	0
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	1	0	1
1	0	0	0	1	0
1	0	0	1	0	0
1	0	1	0	0	1
1	0	1	1	1	0
1	1	X	X	X	X

(ii)



[15 Points]

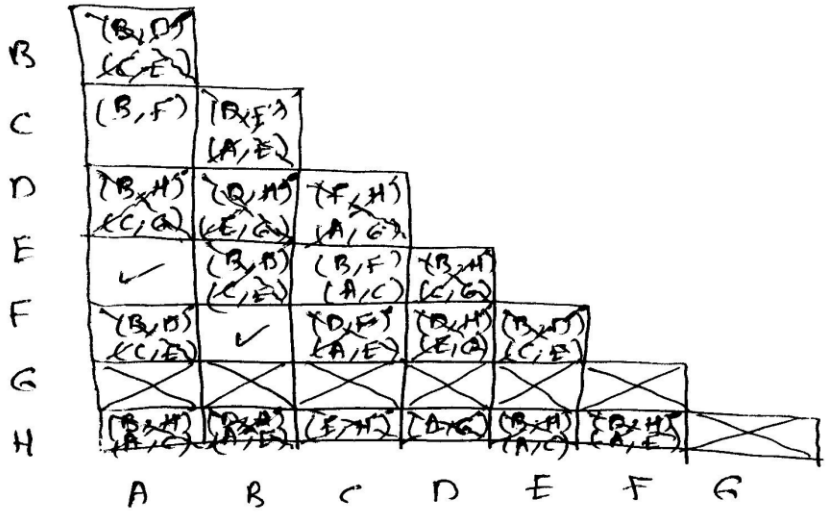
(Q2) Consider the given FSM that has 8 states, one input (X) and one output (Z), represented by the following state table:

Present State	Next State, Z	
	X=0	**X=1**
A	B, 0	C, 0
B	D, 0	E, 0
C	F, 0	A, 0
D	H, 0	G, 0
E	B, 0	C, 0
F	D, 0	E, 0
G	F, 1	A, 0
H	H, 0	A, 0

(i) Determine the equivalent states.

(ii) Reduce the state table into the minimum number of states and show the reduced state table.

(i)



Equivalent States :

(A, C, E), (B, F), (D), (G), (H)

(ii) Let S1 = (A, C, E), S2 = (B, F),

S3 = D, S4 = G, S5 = H

Reduced state table:

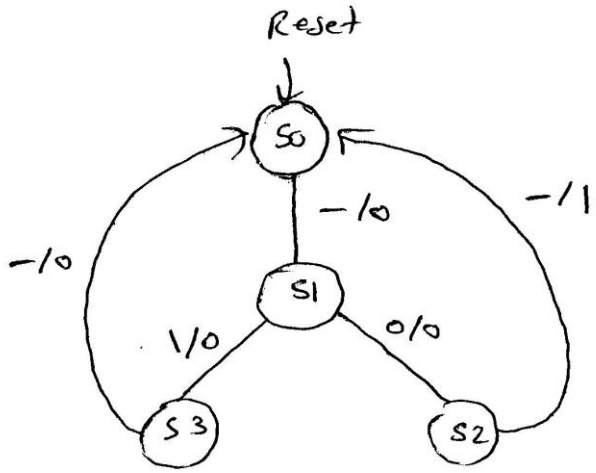
P.S.	N.S., Z	
	x = 0	x = 1
S1	S2, 0	S1, 0
S2	S3, 0	S1, 0
S3	S5, 0	S4, 0
S4	S2, 1	S1, 0
S5	S5, 0	S1, 0

[10 Points]

(Q3) It is required to design a synchronous sequential circuit that receives a sequence of 3-bit nunbers serially through input **X** and produces 1 through output Z when the 3-bit numbers are equal to 000, 001, 100 or 101. Assume the existence of an asynchrnous reset input to reset the machine to a reset state. Draw the state diagram of the circuit assuming a **Mealy** model with **minimum** number of states.. *You are not required to derive the equations and the circuit*. The following is an example of some input and output streams:

Example:

Input	**X**	1 0 1 0 1 0 1 0 0 0 1 0 0 0
Output	**Z**	0 0 1 0 0 0 0 0 1 0 0 1 0 0 1



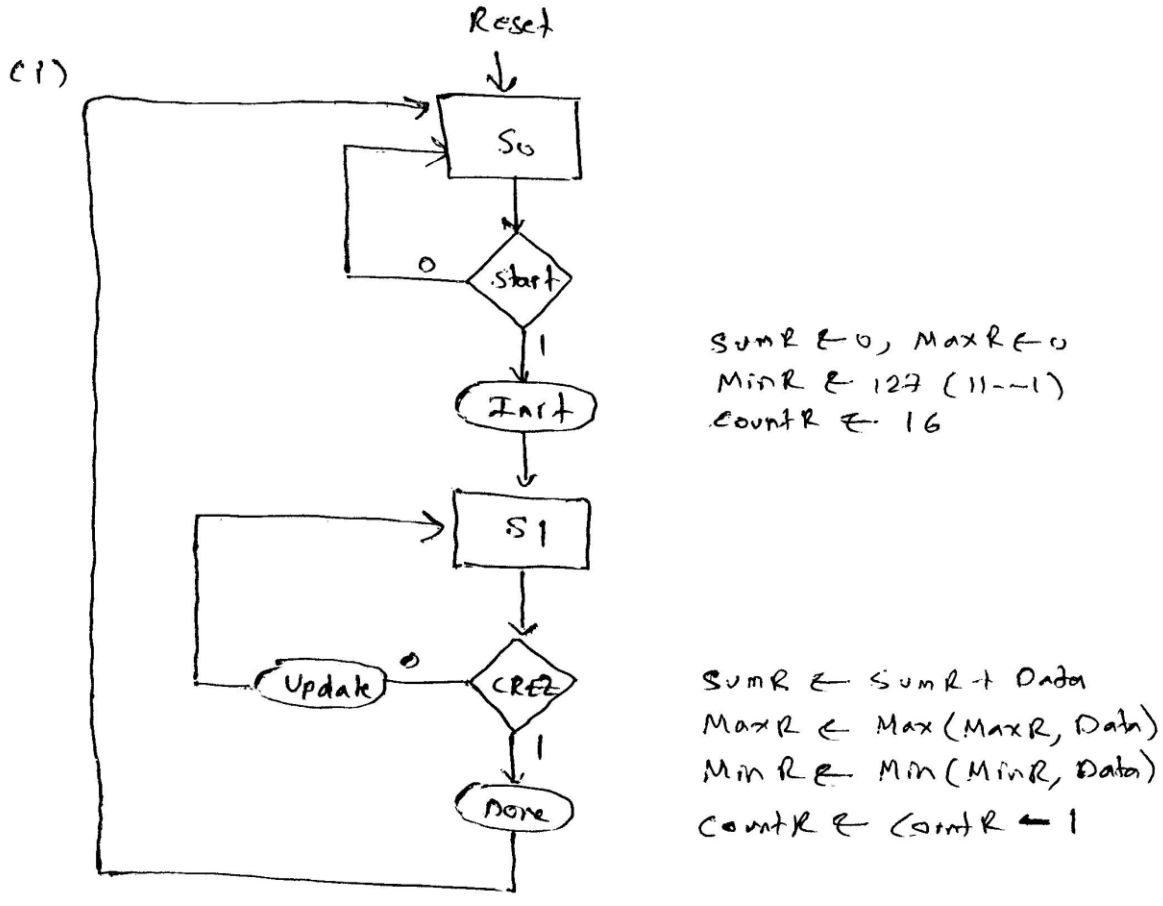
[40 Points]

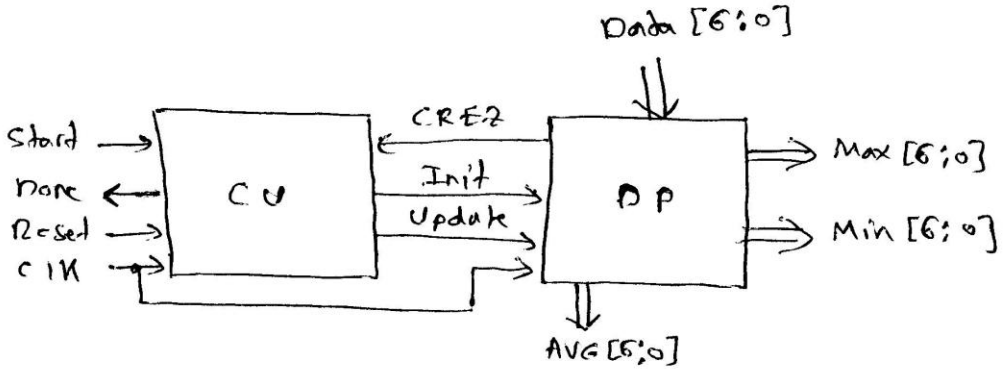
(Q4) It is required to design a circuit that computes the **average**, **maximum** and **minimum** of 16 scores. It is assumed that each score has a value in the range [0,100]. The scores will be fed to the circuit one score at a time the next cycle following the assertion of a *Start* input. Once the circuit finishes computation, it will assert a *Done* signal and will generate the average, maximum and minimum scores. The average will be shown as integer number resulting from dividing the sum by 16 with rounding the result to the nearest integer. Assume the existence of an asynchrnous reset input to reset the machine to a reset state

(i) Develop an ASMD chart for the circuit.

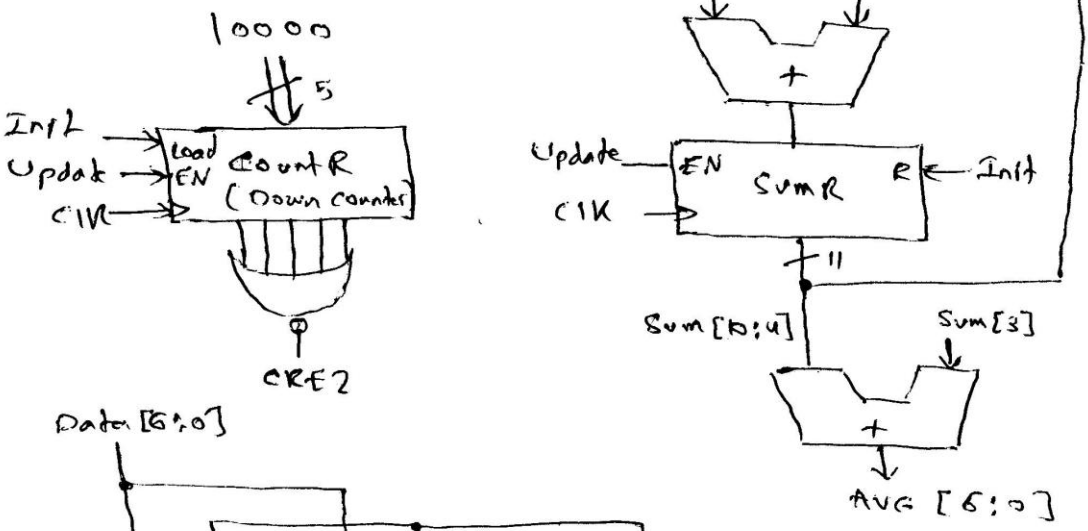
(ii) Show the design of the datapath unit of the circuit. You can use functional blocks such as Adder, Magnitude Comparator, Counter and Multiplexor as blocks without showing their internal details.

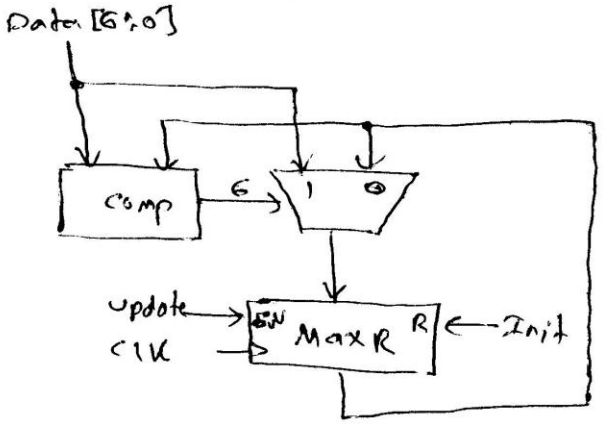
(iii) Show the design and implementation of the control unit of the circuit.

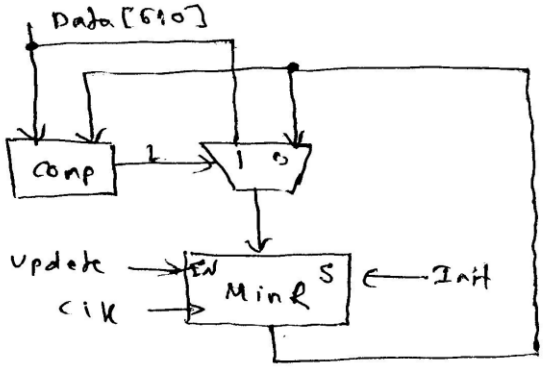



Data [6:0]
Start
Done
Reset
CLK
CU
CREZ
Init
Update
DP
Max [6:0]
Min [6:0]
AVG [6:0]

(ii) Data Path :


10000
5
Init
Update
CLK
Load
EN
Count R
(Down counter)
CREZ
{0000, Data[6:0]}
+
Update
EN
Sum R
R
Init
CLK
11
Sum [6:4]
Sum [3]
+
AVG [6:0]

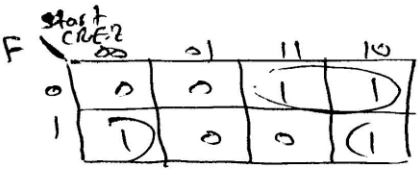

Data [6:0]
Comp
6
1
0
Update
CLK
EN
Max R
R
Init



(III) Control Unit:

C.S.	Start	CREZ	N.S.	Init	Update	Done
S0	0	—	S0	0	0	0
S0	1	—	S1	1	0	0
S1	—	0	S1	0	1	0
S1	—	1	S0	0	0	1

Let S0 = 0 and S1 = 1

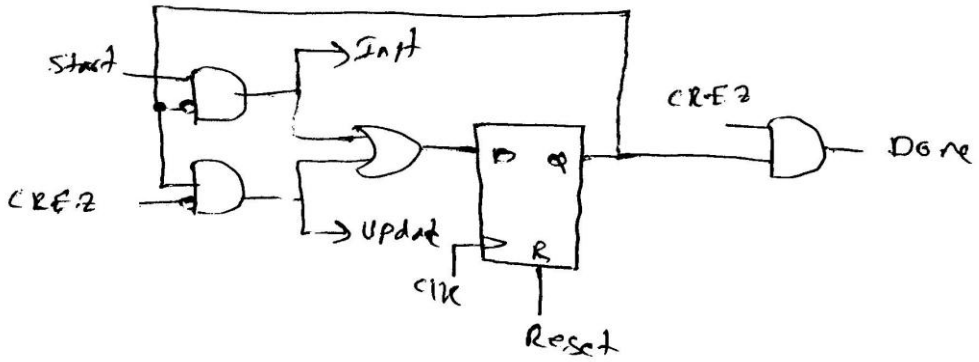


$F^{+} = \bar{F}\,Start + F\,\overline{CREZ}$

$Init = \bar{F} \cdot Start$

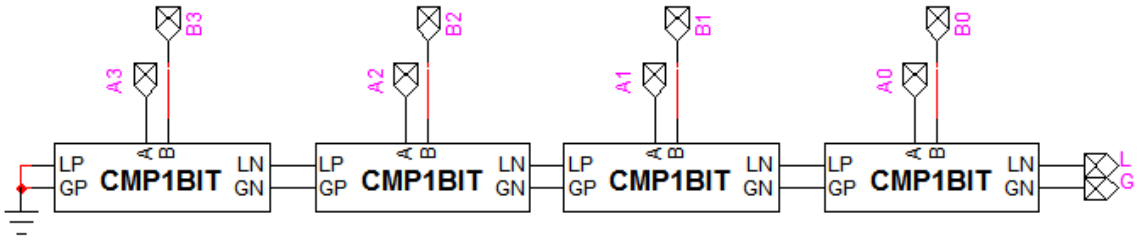
$Update = F \cdot \overline{CREZ}$

$Done = F \cdot CREZ$

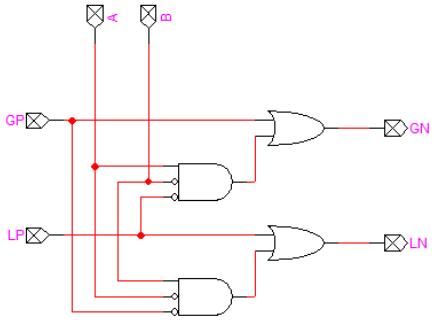


[15 Points]

(Q5) It is required to model a 4-bit iterative magnitude comparator shown below:



The model for a 1-bit comparator is as follows:



Assume that the delay of gates is related to the number of its inputs i.e the delay of an inverter is 1, the delay of a 2-input gate is 2 and the delay of a 3-input gate is 3.

(i) Write a Verilog model for modeling a 1-bit comparator incorporating the given delay information.

(ii) Write a Verilog model for modeling the 4-bit magnitude comparator using the 1-bit comparator model in (i).

(iii) Write a test bench to apply inputs that will result in the longest delay on the outputs of the 4-bit magnitude comparator.

(i)

```
module OneBitCmp (output  GN, LN, input A, B, GP, LP);

not #1 (AB, A);
not #1 (BB, B);
not #1 (GPB, GP);
not #1 (LPB, LP);
and #3 (G1, A, BB, LPB);
and #3 (G2, AB, B, GPB);
or #2 (GN, GP, G1);
or #2 (LN, LP, G2);

endmodule
```

(ii)

```
module FourBitCmp (output  G, L, input [3:0] A, B);

    OneBitCmp C0 (G3, L3, A[3], B[3], 0, 0);
    OneBitCmp C1 (G2, L2, A[2], B[2], G3, L3);
    OneBitCmp C2 (G1, L1, A[1], B[1], G2, L2);
    OneBitCmp C3 (G, L, A[0], B[0], G1, L1);

endmodule
```

(iii)

The longest delay across the 4-bit comparator is 12 ns when the result changes from larger to smaller from the most significant bit and vice versa.

```
module t_FourBitCmp ();

    wire G, L;
    reg [3:0] A, B;
    FourBitCmp M1 (G, L, A, B);
    initial #150 $finish;

    initial begin
    A=8; B=0;
    #15 A=0; B=8;
    #15 A=8; B=0;
    end

endmodule
```