KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 405 Design and Modeling of Digital Systems

Term 152 Lecture Breakdown

Lec #	Date	Topics	Ref.
1	U 17/1	Syllabus & Course Introduction. Introduction to Digital Design Methodology.	Chapter 1
2	T 19/1	Digital System Design Cycle, Architecture Design Example.	Chapter 1
3	TH 21/1	Design Space and Evaluation Space, Digital System Complexity. Dealing with Design Complexity, Design Hierarchy, Abstractions, Design Domains & Levels of Abstraction, Design Methods.	Chapter 1
4	U 24/1	Design vs. Synthesis, Synthesis Process, Circuit Synthesis, Hardware Description Languages, Design Automation & CAD Tools. Definitions: implicant, Prime Implicant, Essential Prime Implicant.	Chapter 1
5	T 26/1	Minimum cover, Minimal cover or irredundant cover. Sum of Product (SOP) Simplification Procedure.	Chapter 2
6	TH 28/1	Shannon's Expansion, Boolean Expansion Based on Orthonormal Basis. Don't Care Conditions.	Chapter 2
7	U 31/1	SOP Simplification Procedure using Don't Cares, Product of Sum (POS) Simplification. Combinational Circuits Design Procedure, Iterative Design.	Chapter 2
8	T 2/2	Decoders, Implementing Functions using Decoders. Multiplexers, Implementing Functions using Multiplexers. Using Adder for comparing signed and unsigned numbers. Sequential Circuit Model.	Chapter 2 & 3
9	TH 4/2	Timing of Sequential Circuits, Latches and Flip-Flops, Sequential Circuit Design Procedure. Sequential Circuit Design Examples.	Chapter 3
10	U 7/2	Sequential Circuit Design Examples.	Chapter 3
11	T 9/2	State Minimization.	Chapter 3
12	TH 11/2	State Minimization, Retiming. **(Quiz#1)**	Chapter 3

13	U 14/2	Retiming, Sequential Circuit Timing, Timing Constraints, FF set up time, Clock to Q delay, FF hold time, Clock Skew, Peak to Peak Jitter, Hold Time violation, metastability, synchronizing flip-flops.	Chapter 3
14	T 16/2	Data Path & Control Unit Partitioning, Data Path Design, Registers, Shift Registers, Modulo N (i.e. divide by N) Counters. Counters as Clock frequency dividers.	
15	TH 18/2	Three-State Devices, A Register Bank with a 4-bit Data Bus, Design Steps. Digital System Design Example: Traffic Light Controller.	
16	U 21/2	Digital System Design Example: Traffic Light Controller. Algorithmic State Machine (ASM) Chart, Timing in ASM Charts.	5.14-5.15
17	T 23/2	ASM Chart => Controller, ASM Chart => Architecture/Data Processor, Implementing Controller, Algorithmic State Machine and DataPath (ASMD) Chart, ASMD Chart for 4-bit Counter. 2:1 Decimator.	5.14-5.15
18	TH 25/2	Implementation of Data Path and Control Unit from ASMD Chart: 2:1 Decimator, One's Count Circuit.	5.14-5.15
	TH 25/2	**Last Day for Dropping with W**	
19	U 28/2	Implementation of Data Path and Control Units of One's Count Circuit. **(Quiz#2)**	5.14-5.15
20	T 1/3	Solution of Quiz#2.	
21	TH 3/3	ASMD Chart Examples: Scores Avg., Max. & Min., Average Computation of Serial Data.	5.14-5.15
	S 5/3	**Midterm Exam**	
22	U 6/3	Introduction to Verilog, Why use HDL?, Definition of a Module. Gate-level modeling, Verilog primitives.	4.1-4.2
23	T 8/3	Verilog Syntax, Verilog Data Types. Module instantiation.	4.1-4.2
24	TH 10/3	Organization of a Testbench for Verifying a Unit Under Test (UUT), Testbench Template, Propagation Delay, Inertial Delay	4.2-4.4
	13-17/3	**Midterm Vacation**	
25	U 20/3	Data Types for Behavioral Modeling, Boolean Equation-Based Behavioral Models of Combinational Logic, Assign Statement, Verilog Operators.	5.1-5.3
26	T 22/3	Propagation Delay & Continuous Assignment, Always Block, Procedural Assignment, Wire vs. Reg, Algorithm-Based Models, if statement, Case statement.	5.4-5.6
27	TH 24/3	Introduction to using Xilinx Tools and Boards.	

28	U 27/3	Case statement, Behavioral Models of Multiplexor, Encoder, Decoder. D Latch, D Flip-flop (synchronous & asynchronous reset),	5.6-5.9
29	T 29/3	Data Flow/ RTL Models: Shifter. Behavioral Models of Multiplexor. Encoder, Decoder. Seven Segment Display Decoder, Linear Feedback Shift Register (LFSR),	5.6-5.11
30	TH 31/3	LFSR Modeling, Repetitive Algorithms: for loop. Parametrizable ripple carry adder using for loop.	5.9-5.11
	TH 31/3	**Last Day for Dropping all Courses with W**	
31	U 3/4	Repetitive Algorithms: repeat loop, while loop, disable, forever. Tasks and Functions. (**Quiz#3**)	5.11-5.13
32	T 5/4	Behavioral Modeling of Control Unit, Behavioral Models of Counters. Behavioral Models of Shift Registers. Barrel Shifter, Universal Shift Register, Register Files, File I/O system functions and tasks.	5.14-5.16
33	TH 7/4	File I/O system functions and tasks. Circuit Synthesis, Multilevel logic synthesis, Logic Network modeling, Network Optimization, Area and Delay estimation, Relation between testability and redundancy, Multilevel Logic Transformations: Elimination.	6.1
34	U 10/4	Multilevel Logic Transformations: Elimination, Decomposition, Factoring, Extraction, Simplification, Substitution. Synthesis & Testability.	6.1
35	T 12/4	Synthesis & Testability.	6.1
36	TH 14/4	Timing Issues in Multiple-Level Logic Optimization . (**Quiz#4**)	6.1
37	U 17/4	Network Delay Modeling, topological critical path, false path, Algorithms for Delay Minimization, Behavioral or High-Level Synthesis: CDFG, scheduling, allocation.	6.1
38	T 19/4	Behavioral or High-Level Synthesis: CDFG, scheduling, allocation.	6.1
39	TH 21/4	Tutorial on using LCD Screen.	
40	U 24/4	(**Quiz#5**)	
41	T 26/4	Solution of Quiz#5, Synthesis of Combinational Logic.	6.1-6.6
42	TH 28/4	Synthesis of Priority Structures. Exploiting Logical Don't Care Conditions, Resource Sharing, Synthesis of Sequential Logic with Latches. Using Xilinx IP CoreGen Tool.	6.1-6.6
	TH 28/4	**Dropping all Courses with WP/WF**	

43	U 1/5	Synthesis of Three-State Devices and Bus Interfaces, Synthesis of Sequential Logic with Flip-Flops. Synthesis of Explicit State Machine. Synthesis of Gated Clocks and Clock Enable, Operator Grouping, Expression Substitution, Synthesis of loops. Programmable Logic and Storage Devices: History of Computational Fabrics, ASIC vs. FPGA, FPGA Advantages, Reconfigurable Logic, Anti-Fuse-Based Approach.	6.1-6.6 Chapter 8
44	T 3/5	RAM Based Field Programmable Logic, Xilinx FPGA Families, The Xilinx 4000 CLB. LUT Mapping, Configuring the CLB as a RAM, FPGA Interconnect, Basic I/O Block Structure, CLB Structure, 5-Input Functions, Distributed RAM, Shift Register, Carry & Control Logic.	Chapter 8
45	TH 5/5	Adder Implementation, Carry Chain, 18 x 18 Embedded Multiplier. FPGA Design Flow – Mapping, Placement & Route. Memory Types, FPGA Memory Implementation, LUT-Based RAMS, Block RAM. Block RAM Logic Diagram, Block RAM Data Combinations and ADDR Locations, Read & Write Operations, Write Modes, Conflict Avoidance, Using Core Generator.	Chapter 8