COE 405, Term 162

Design & Modeling of Digital Systems

Assignment# 5

Due date: Saturday, May 13

Q.1. Consider the following function:

X=AC+BC+AD+BD+A'B'C'+A'B'D'+AEF+BEF+AE'F'+BE'F'+A'B'EF'+ A'B'E'F

(i) Compute all double-cube divisors of *X* along with their bases and their weights. Show only double-cube divisors that have non-empty bases.

(ii) Apply the fast extraction algorithm based on extracting double-cube divisors along with complements or single-cube divisors with two-literals. Show all steps of the algorithm. Determine the number of literals saved. Compare your solution with the result obtained by running the sis commands ***fx***.

Q.2. Consider the logic network defined by the following expressions:

e=a b d

f =c d

g = e + f

h = a d

i =a' b' d'

j = h + i

k= b d

l =j + k

x =g + l

Inputs are {a, b, c, d} and output is {x}. Assume that the delay of a gate is related to the number of its inputs. Also, assume that the input data-ready times are zero except for input d, which is equal to 2.

(i) Draw the logic network graph and compute the data ready times and slacks for all vertices in the network.

(ii) Determine the **maximum propagation delay** and the **topological critical path**.

(iii) Suggest an implementation of the function ***x*** to reduce the delay of the circuit. What is the **maximum propagation delay** after the modified implementation?

Q.3. It is required to design a circuit to compute the equation Y=A+2*B+3*C, where A, B, and C are N-bit inputs representing signed numbers in 2's complement representation. Assume that inputs are available only during the first cycle when a **START** input is asserted. Assume that a **DONE** signal will be set when the result is ready and the result will remain held until the next Start operation.

(i) Show a schedule of the operations with minimum latency (i.e., clock cycles) assuming that the clock cycle is limited by the time for performing one addition operation. Store the output Y in a register.

(ii) Show the Data Path design of your circuit indicating all the control signals and the used adder sizes.

(iii) Show the ASMD diagram of your control unit.

(iv) Write the necessary Verilog modules to module the data path unit, control unit and the overall circuit.

(v) Write a test bench to test the correct operation of your circuit. Include simulation snapshots.

(vi) Implement your circuit on FPGA assuming N=2 bits. Include a link for a video snapshot to demonstrate correct functionality of your circuit.

This assignment can be solved based on a group of two students. The solution should be well organized. Submit a soft copy of your solution in a zip file including your Verilog models. Your solution should be submitted in a ***word file*** *that contains the following items:*

i. Your name and ID

ii. Assignment number

iii. Problem statement

iv. Your solution

v. Include snapshots of simulation output to illustrate the correctness of your models.